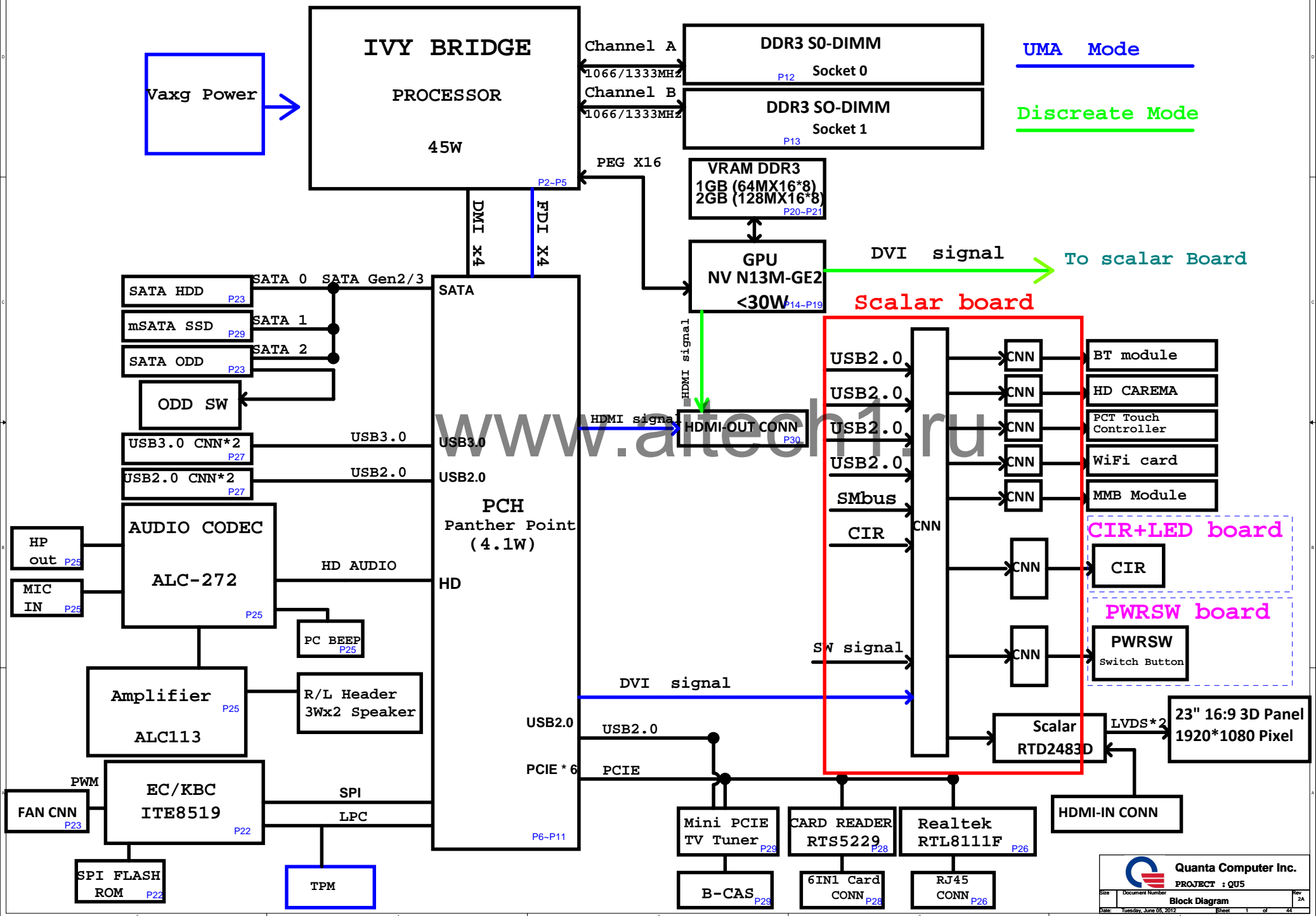


A520-INTEL CHIEF RIVER+ GFX/UMA BLOCK DIAGRAM



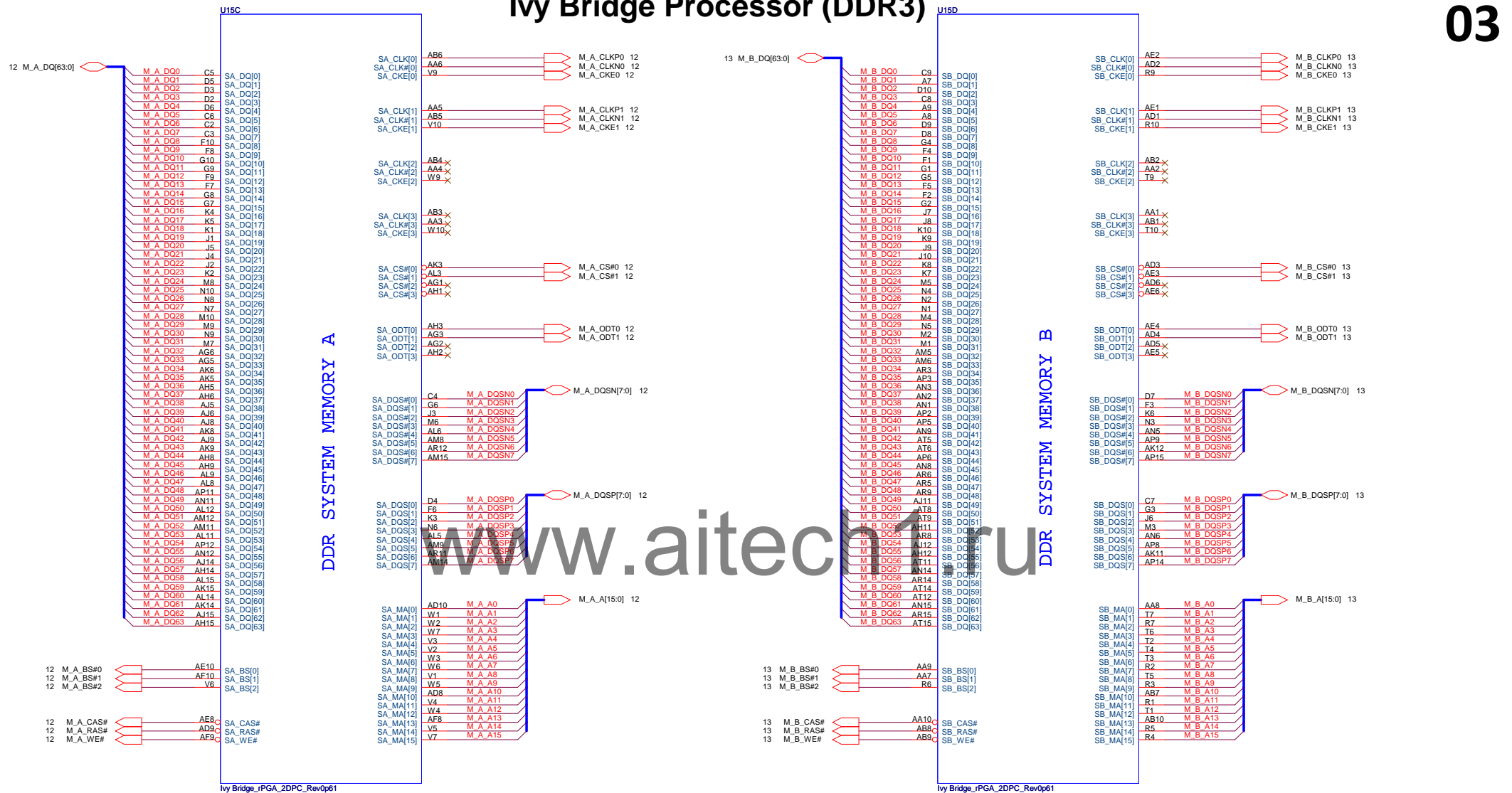


PROJECT : QU5

PEG_ICOMPI and RCOMPO signals
should be routed within 500 mils typical
impedance = 43 mohms PEG_ICOMPO
signals should be routed within 500 mils
typical impedance = 14.5 mohms

0.22uF AC coupling Caps for PCIe GEN3

Ivy Bridge Processor (DDR3)

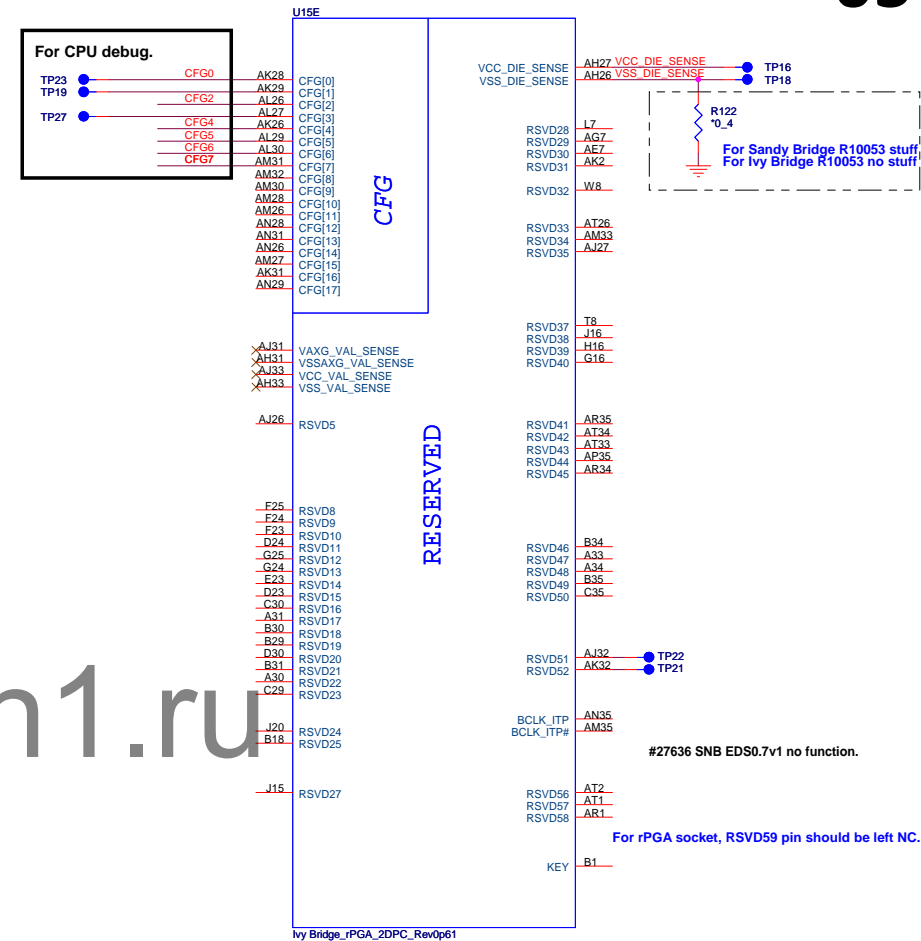


Quanta Computer Inc.

PROJECT : QU5

Size	Document Number	Rev
	SNB 2/4 (DDR3 I/F)	1A

Date: Tuesday, June 05, 2012 Sheet 3 of 44



The CFG signals have a default value of '1' if not terminated on the board

(hh) TWH PEG bus is Lane Reverse

CFG2 R151 1K 4

CFG4 R152 *1K 4

CFG7 R150 *1K 4

CFG5 R143 *1K 4

CFG6 R149 *1K 4

CFG[6:5] (PCIe Port Bifurcation Straps)

```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```



Quanta Computer Inc.

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Size	Document Number	Rev
	SNB 4/4 (GND)	1A
Date:	Tuesday, June 05, 2012	Sheet 5 of 44

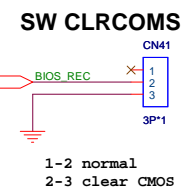
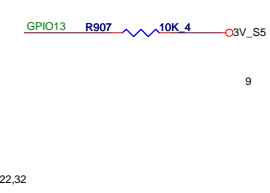
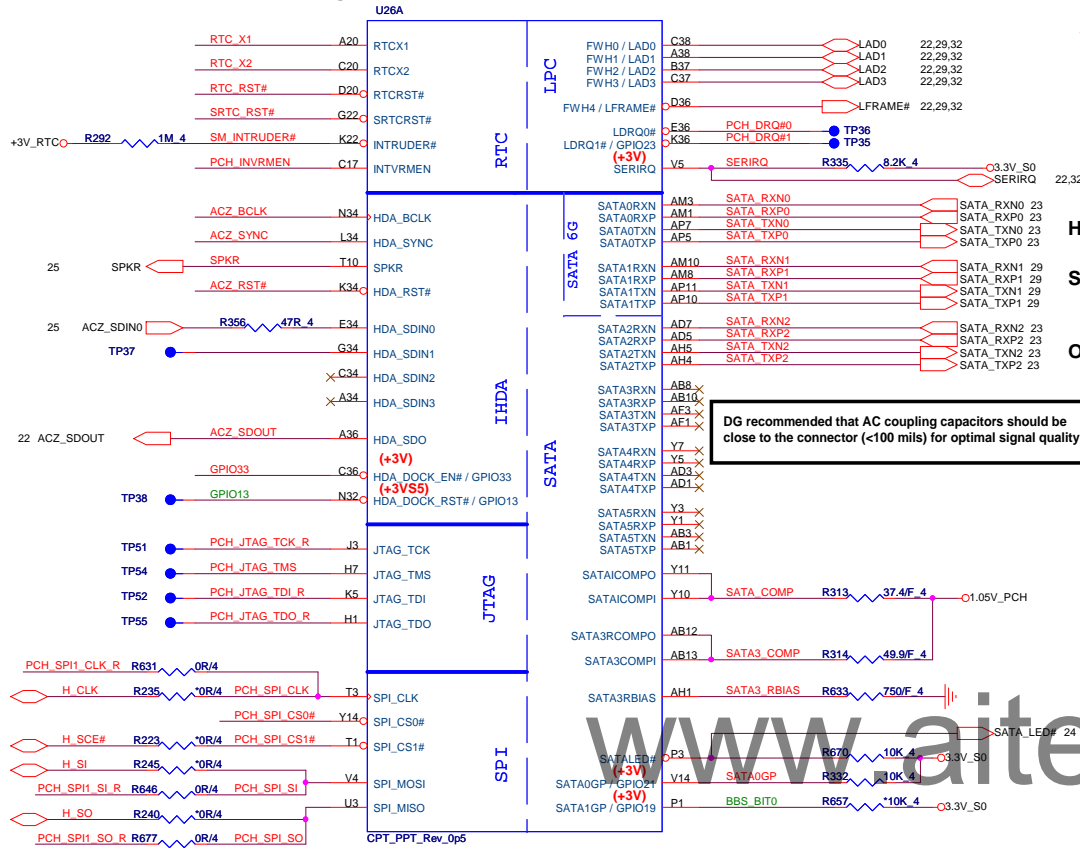
Cougar Point/Panther Point (LVDS,DDI)

U26C



Cougar Point/Panther Point (HDA,JTAG,SATA)

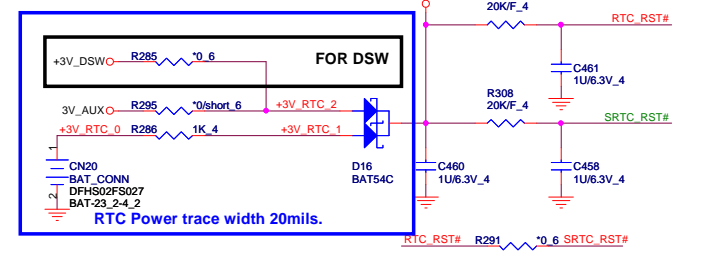
07



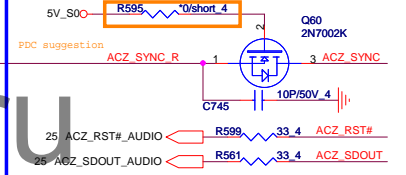
HDD0 (SATA3 6.0Gb/s)
SSD (SATA3 6.0Gb/s)
ODD (SATA1 1.5Gb/s)

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

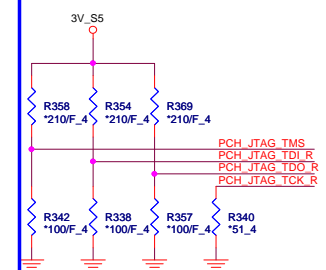
RTC Circuitry(RTC)



HDA Bus(CLG)



PCH JTAG Debug(CLG)

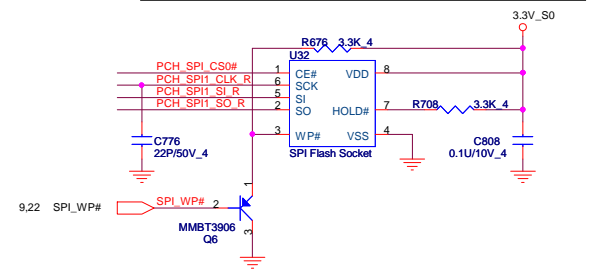


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit										
SPKR	Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)											
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up											
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)											
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>0</td><td>SPI</td></tr><tr><td>0</td><td>1</td><td>LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	1	0	SPI	0	1	LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	
GNT1#	GNT0#	Boot Location												
1	0	SPI												
0	1	LPC												
GPIO19	Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN										
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)											
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm											
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V											
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)											
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)											
GPIO28	Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable											

SPI FLASH (BIOS+ME)

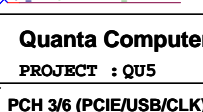
Vender	Size	P/N
MAX		
Winbond	8MB	AKE3EFP0N00 (W25Q64BVSSIG)
Socket		DG008000031



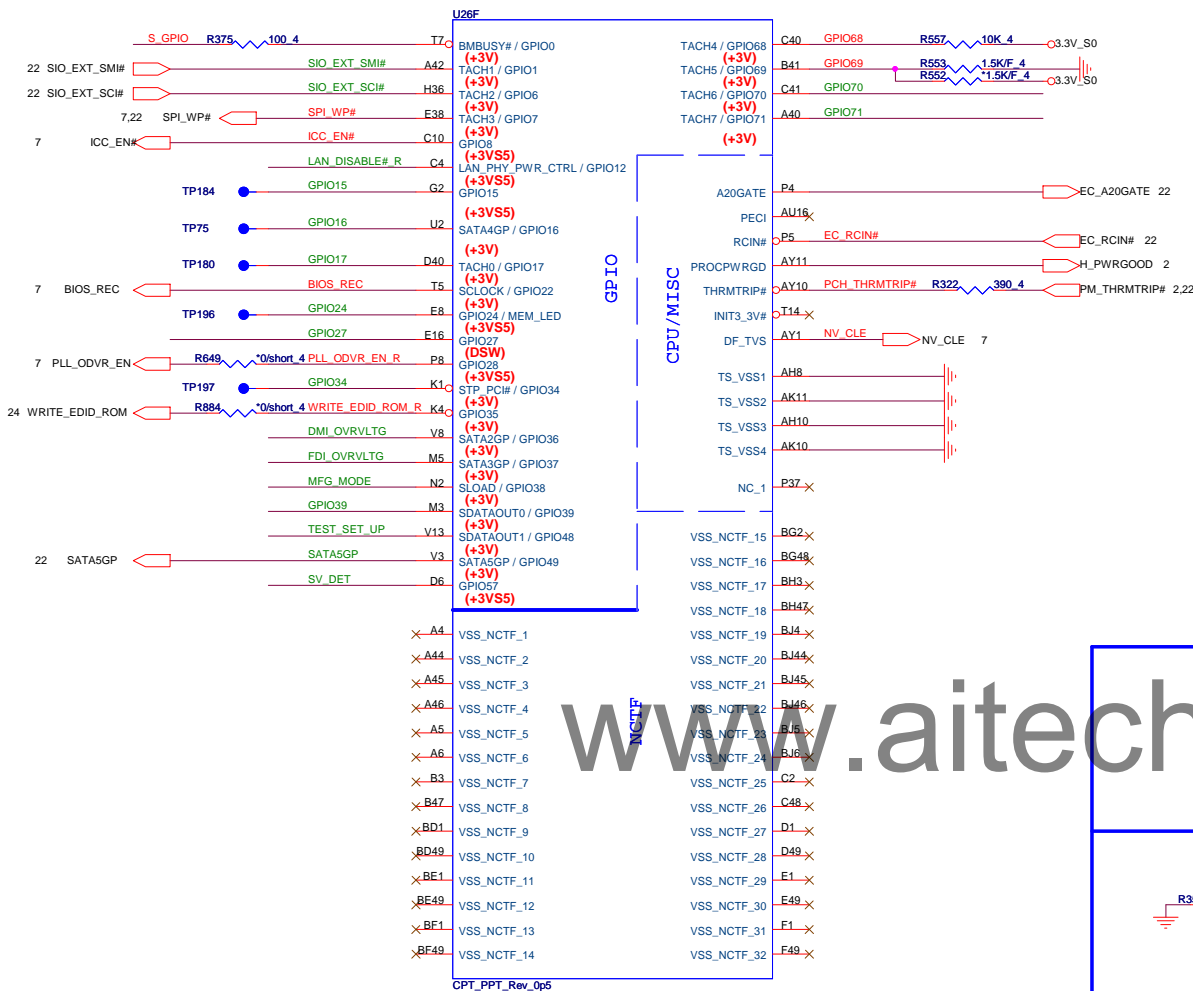
Quanta Computer Inc.
PROJECT : QU5

Size	Document Number	PCH 2/6 (SATA/HDA/SPI)	Rev. 1A
Date:	Tuesday, June 05, 2012	Sheet 7 of 44	

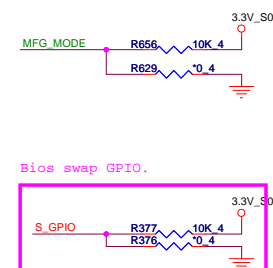
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



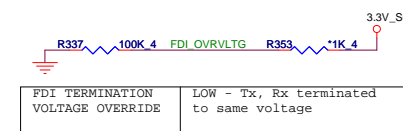
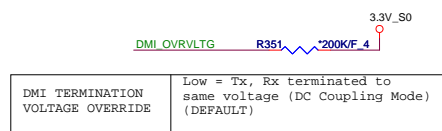
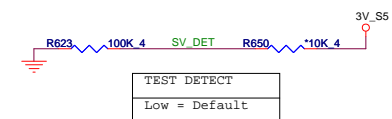
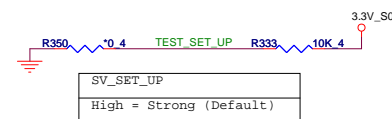
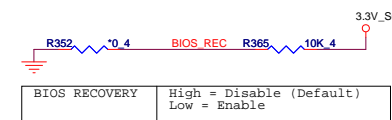
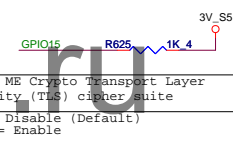
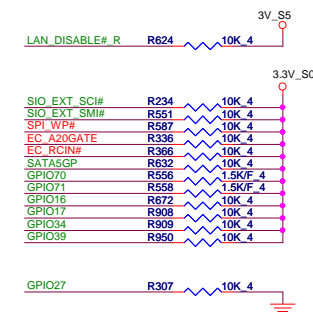
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



MFG-TEST



GPIO Pull-up/Pull-down(CLG)



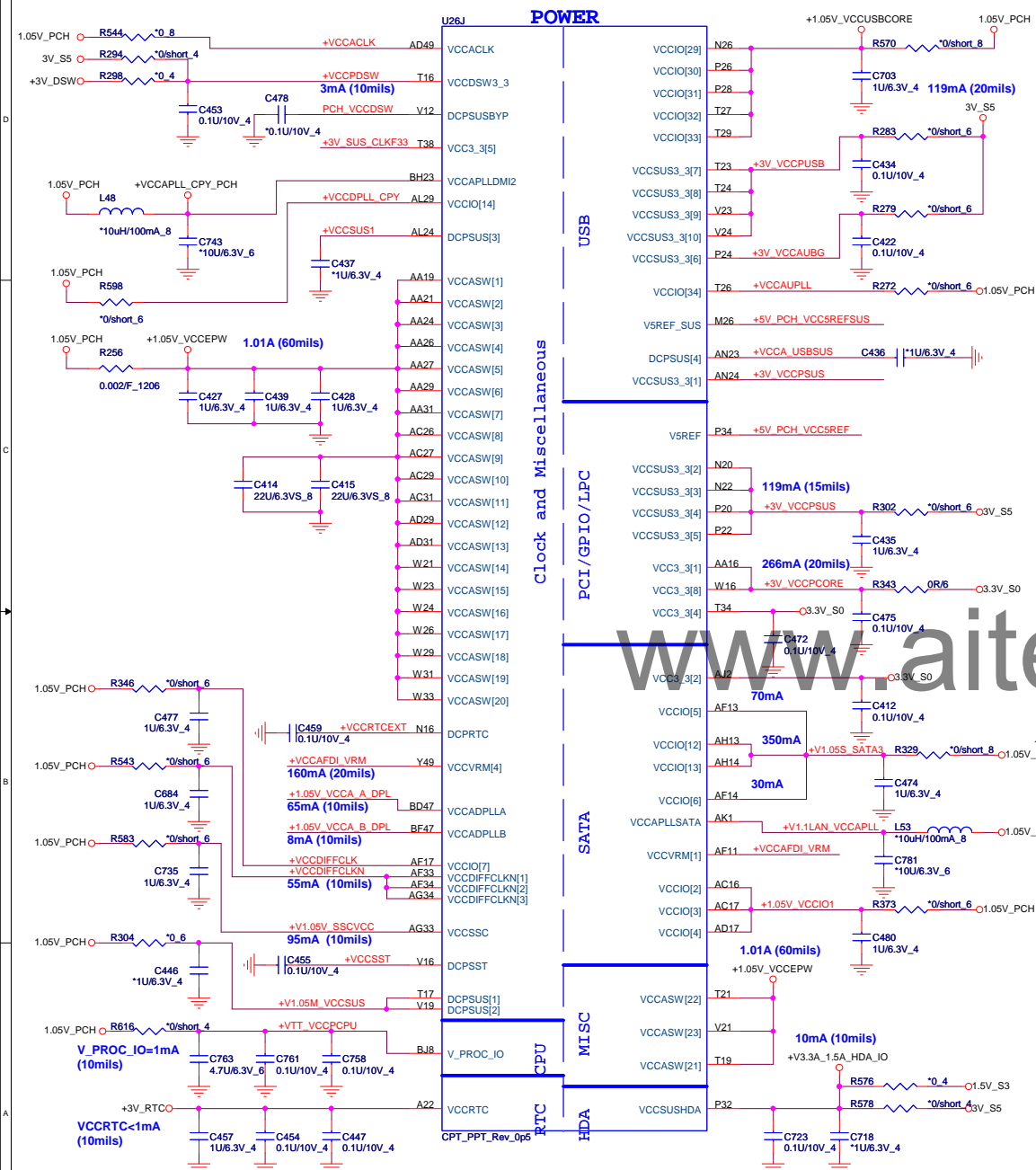
Quanta Computer Inc.

PROJECT : QU5

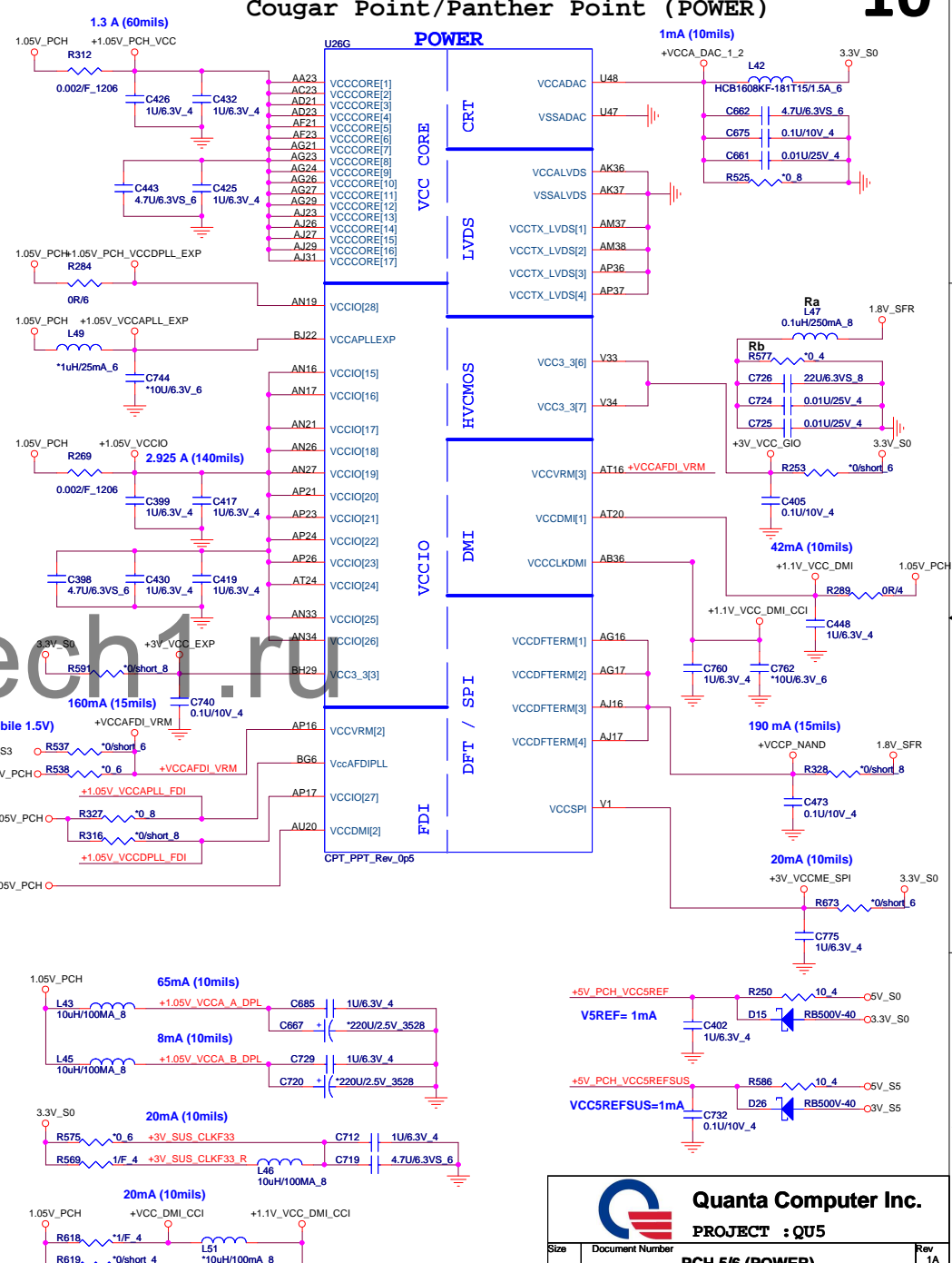
Size Document Number PCH 4/6 (GPIO/MISC) Rev. 1A

Date: Tuesday, June 05, 2012 Sheet 9 of 44

Cougar Point/Panther Point (POWER)

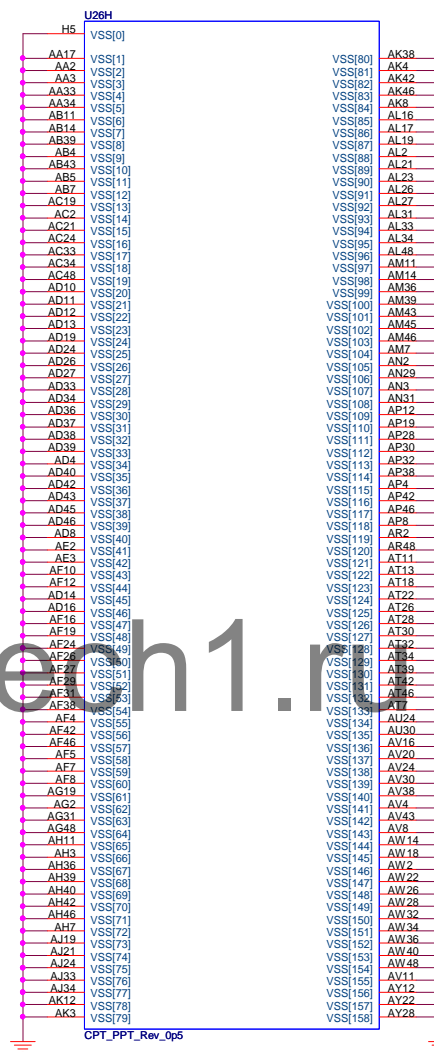
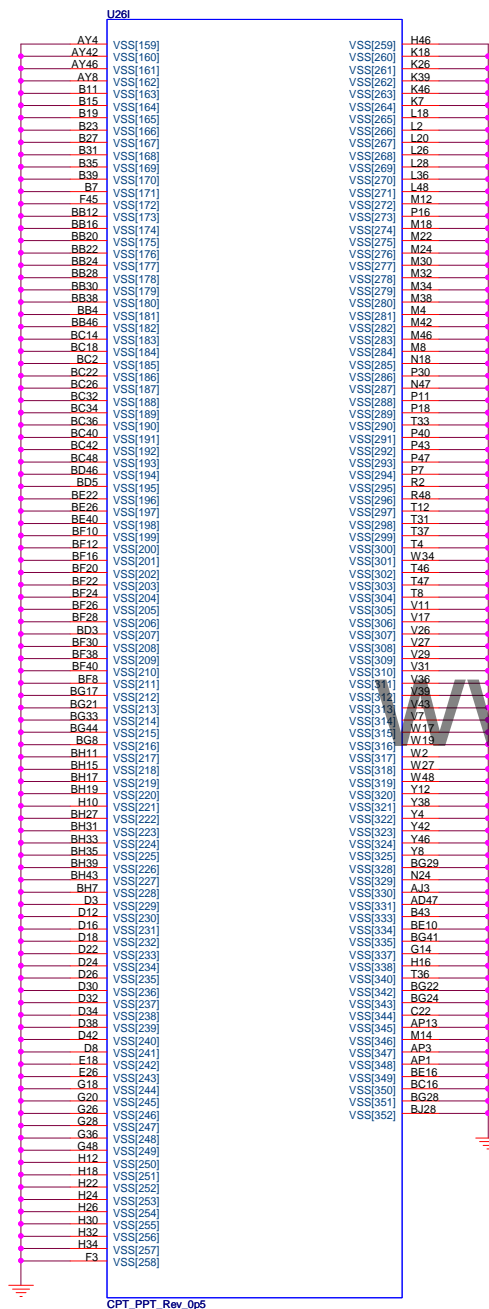


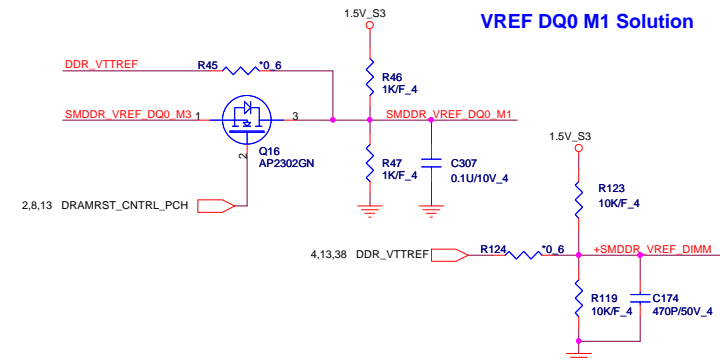
Cougar Point/Panther Point (POWER)

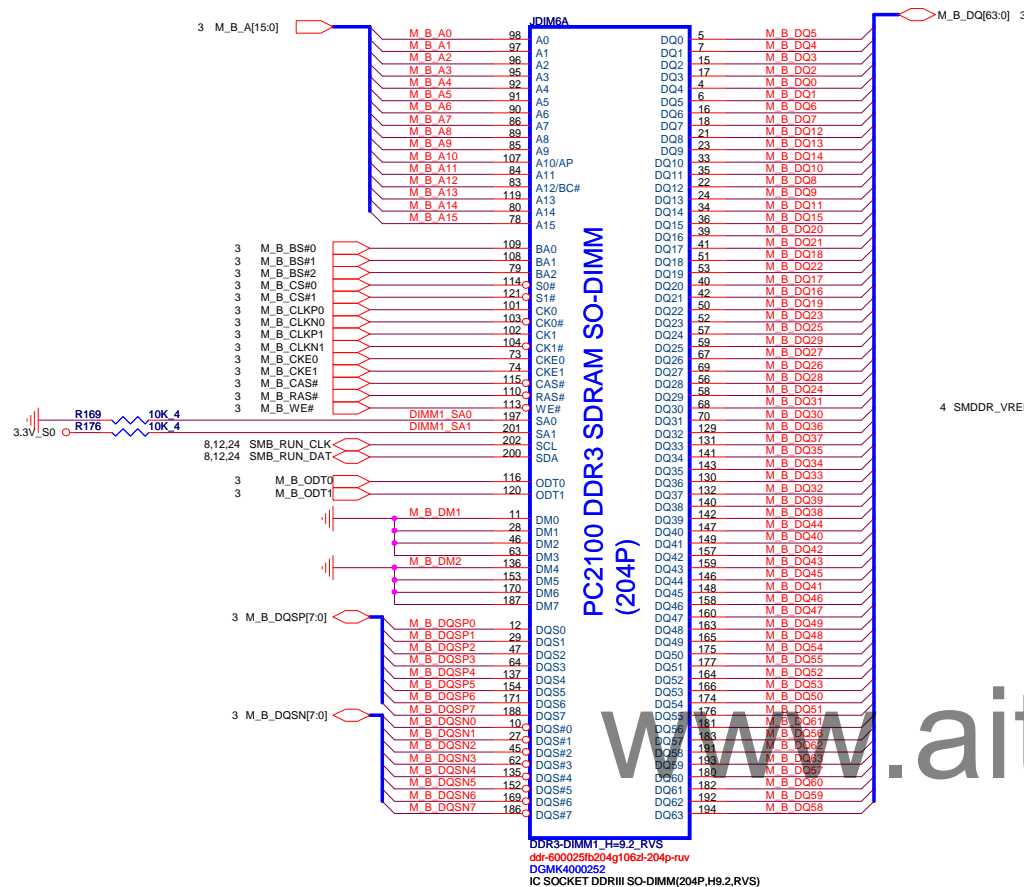


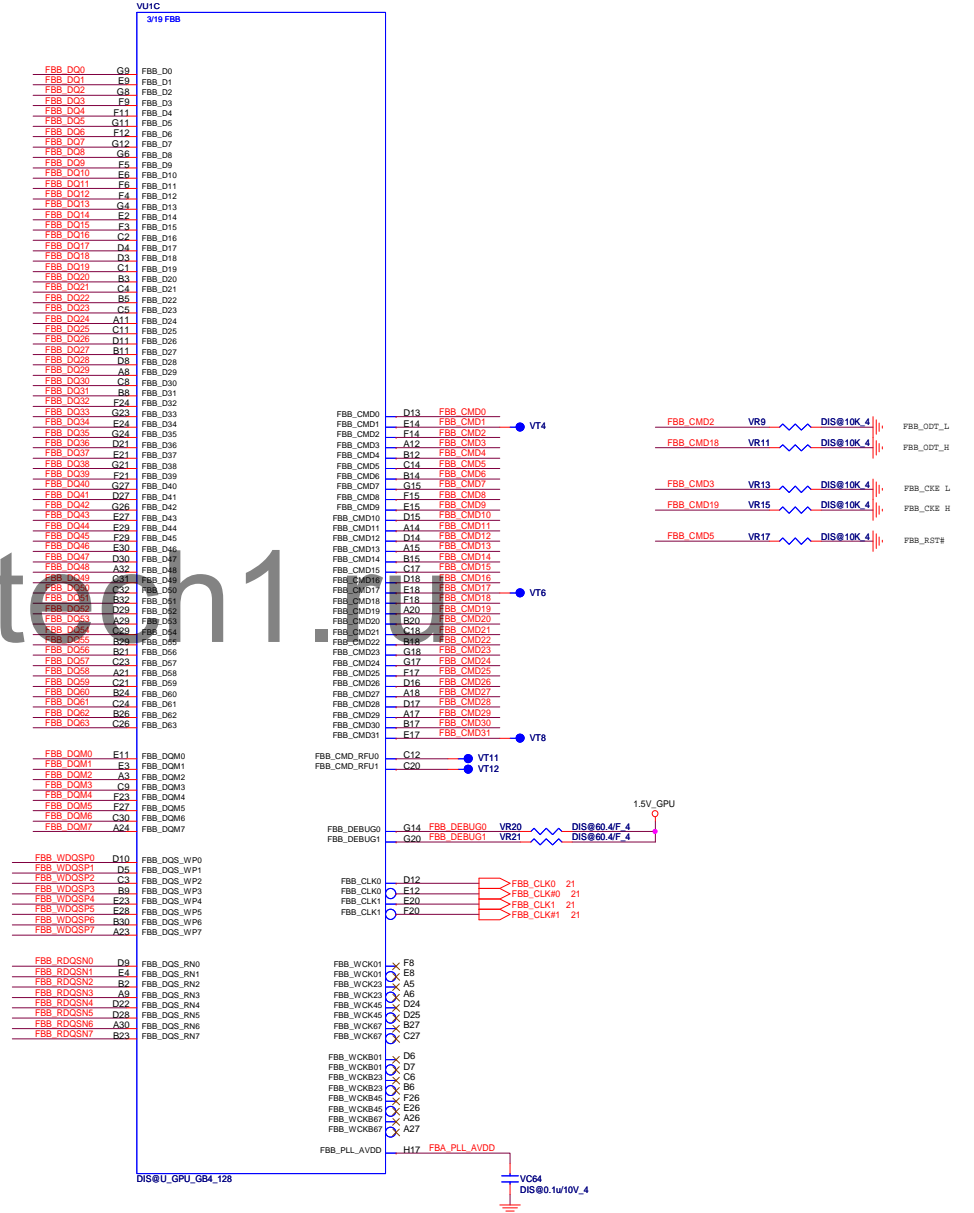
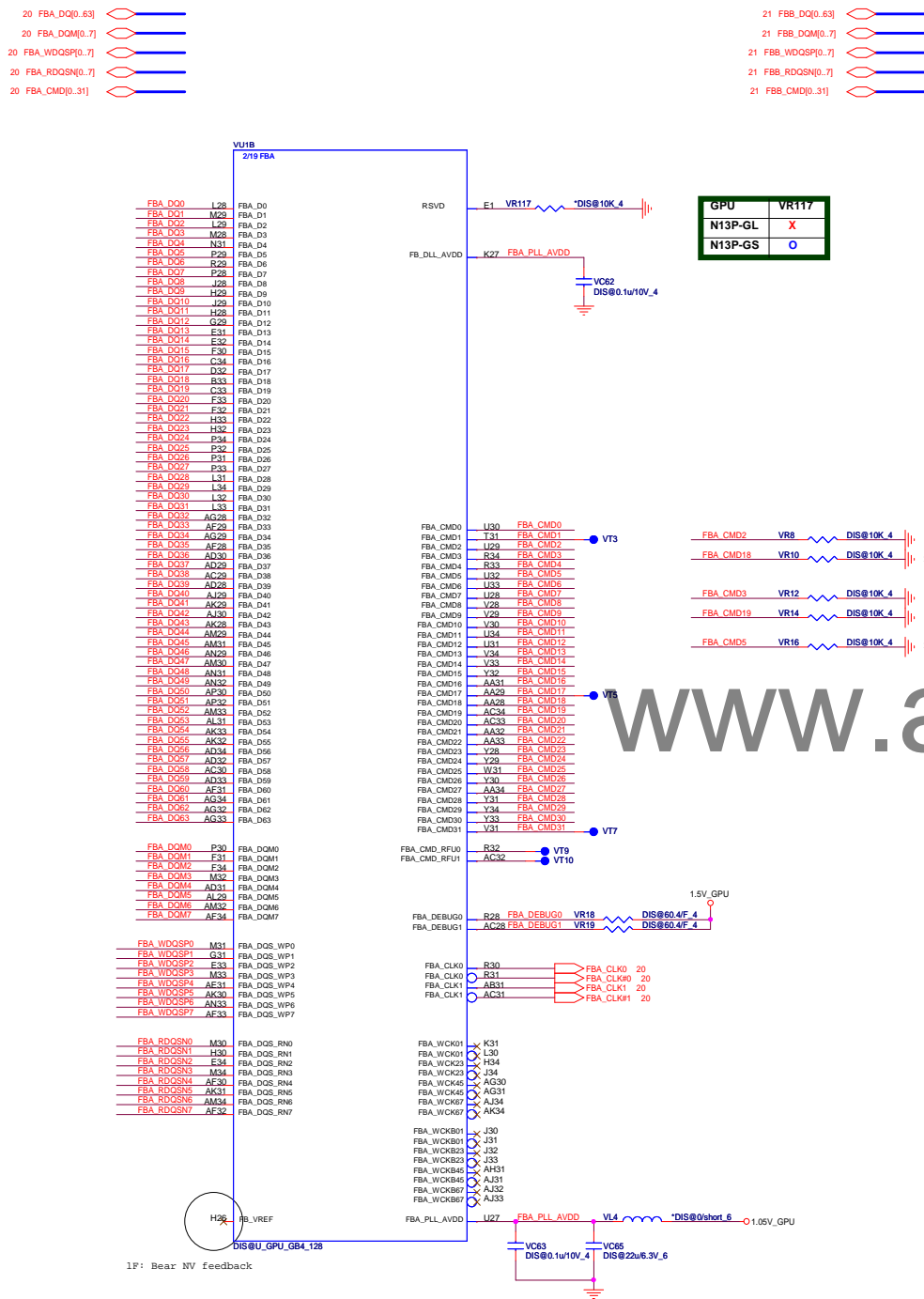
Cougar Point/Panther Point (GND)

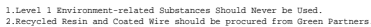
Cougar Point/Panther Point (GND)



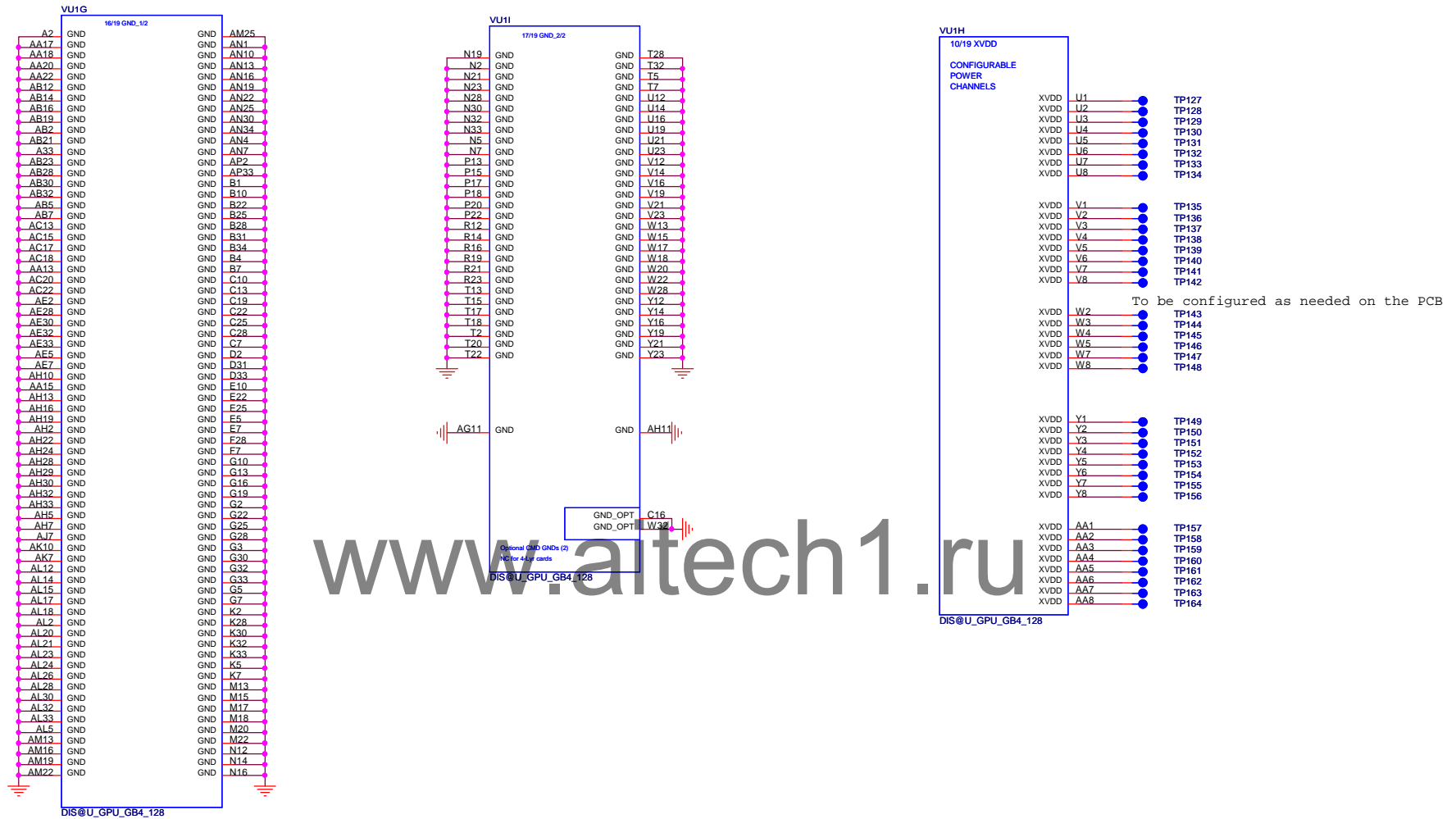










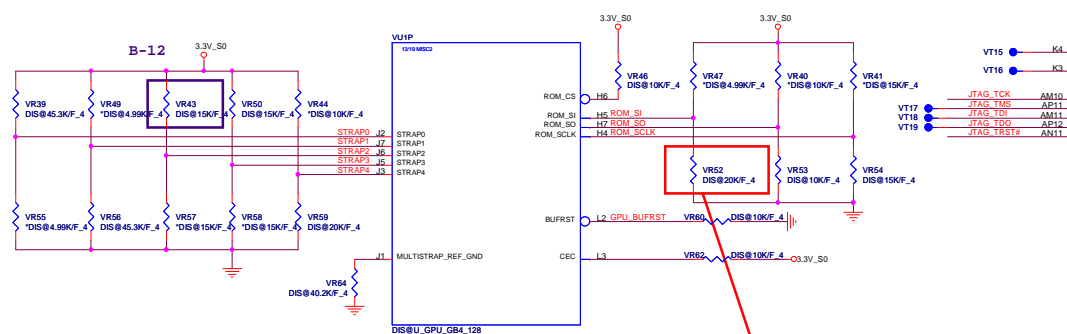


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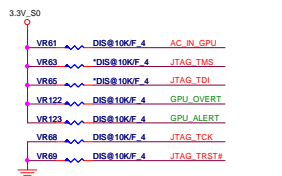
PROJECT : QU5

Size	Document Number	Rev
	N13M-GE2 GND	1A
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1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.



VRAM	VR52
64Mx16 DDR3 Hynix	15K 1%
64Mx16 DDR3 Samsung	20K 1%
128Mx16 DDR3 Samsung	45.3K 1%
128Mx16 DDR3 Hynix	34.8K 1%

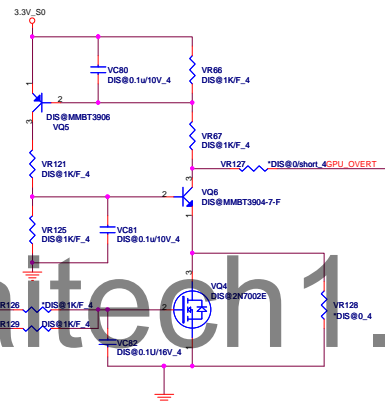


Feedback238(check default setting with NV)

For IVMP 6.5 (GPU)



VID6	VID5	VID4	VID3	VID2	VID1	VID0	Vcc-core
0	1	0	1	1	0	0	0.9500V



Logical Strap Bit Mapping

	PU-VDD	PD	QCI PN(0402)
4.99K	1000	0000	CS24992FB26
10K	1001	0001	CS31002FB26
15K	1010	0010	CS31502FB24
20K	1011	0011	CS32002FB29
24.9K	1100	0100	CS32492FB16
30.1K	1101	0101	CS33012FB18
34.8K	1110	0110	CS33482FB22
45.3K	1111	0111	CS34532FB18

VRAM(DDR3) Configuration Table

RAMCFG [3:0]	DESCRIPTION (Vendor P/N)		Vendor	QCI P/N	ROM_SI	ET SM
0010	64*16-900MHz	H5TG1G63DFR-11C	Hinyx	AKD5LZWTW02	PD 15K	X
0011	64*16-900MHz	K4W1G1648G-BC11	Samsung	AKD5EGG7500	PD 20K	X
0110	128*16-900MHz	H710ZG3838-11K	Hinyx	Reverse	PD 35K	X
0111	128*16-900MHz	K4W2G1648G-HC11	Samsung	Reverse	PD 45.3K	X

N13P-GS/GLP	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417 FB[1]	FB_0_BAR_SIZE FB[0]	SMB_ALT_ADDR	VGA_DEVICE	0101
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG PCI_DEVIDE[5]	PEX_PLL_EN_TERM	1010 0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD03V	0011
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	1010 1111
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1001 1001
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

QS Samples GS:5K PU / GLP:15K PD
ES Samples GS/GLP:15K PU

DG_table111

GF108-ES4 Samples GL:45.3K PU

notebook default
EDID is used

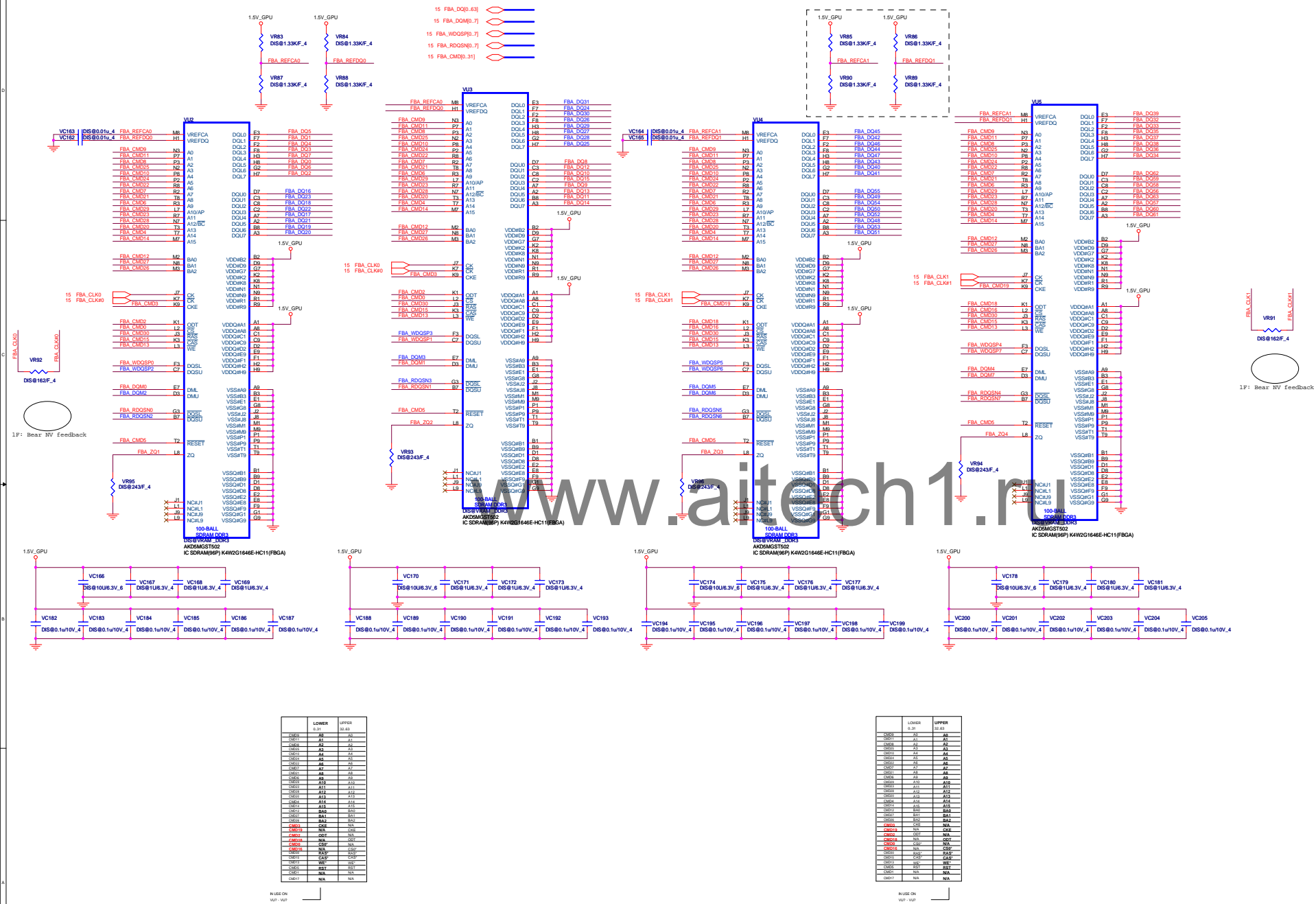
GPIO ASSIGNMENTS

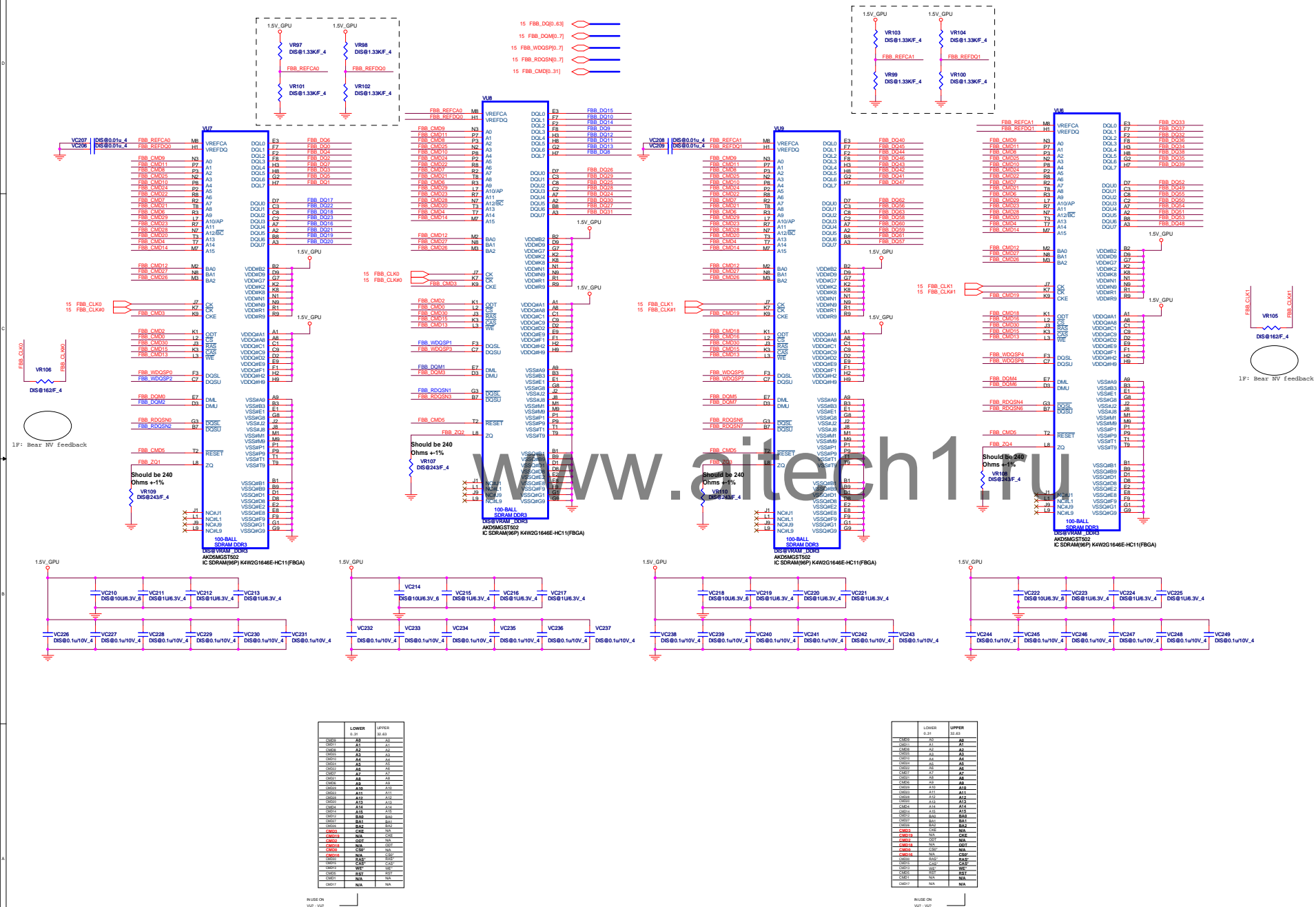
GPIO	I/O	ACTIVE	USAGE
0	OUT	N/A	NVVDD VID4
1	OUT	N/A	NVVDD VID3
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID1
6	OUT	N/A	NVVDD VID2
7	OUT	N/A	3D STEREO
8	I/O	LOW	GPU Overtemp
9	I/O	LOW	GPU ALERT
10	OUT	N/A	FB Vref Control (not used sDDR3)
11	OUT	N/A	NVVDD VID0
12	IN	N/A	PWR_Level AC Detect
13	OUT	N/A	NVVDD VID5
14	IN	N/A	HPD for IFP AB (not used)
15	IN	N/A	HPD for IFP C (HDMI)
16	OUT	N/A	MEM_VDD_CTL
17	OUT	N/A	HPD for IFP D (not used)
18	OUT	N/A	HPD for IFP E (TMDS)
19	OUT	N/A	HPD for IFP F (not used)
20	OUT	N/A	NVGEM Debug GPIOI3
21	OUT	N/A	NVGEM Debug GPIOI4

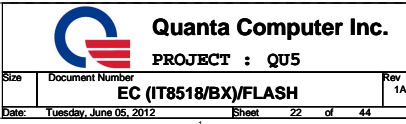
**Quanta Computer Inc.**

PROJECT : QU5

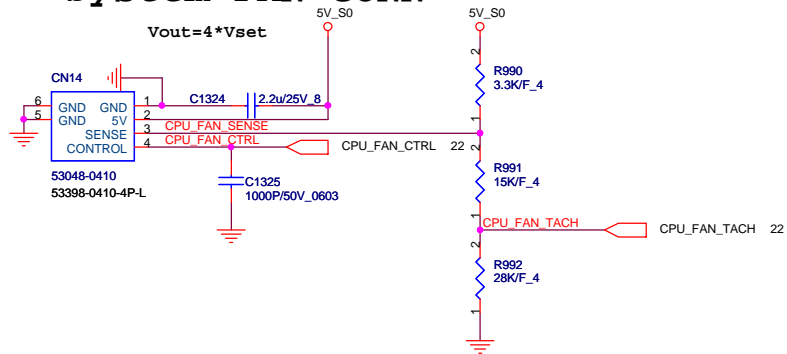
N13M-GE2 STRAP/GPIO



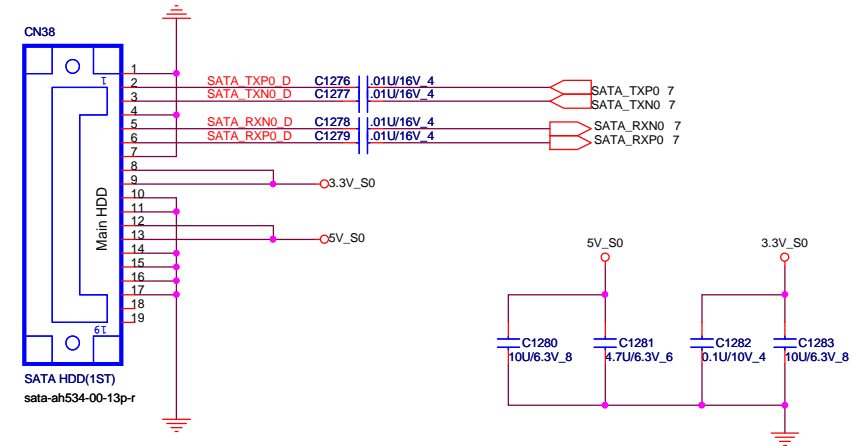




System FAN CONN



SATA HDD CONN

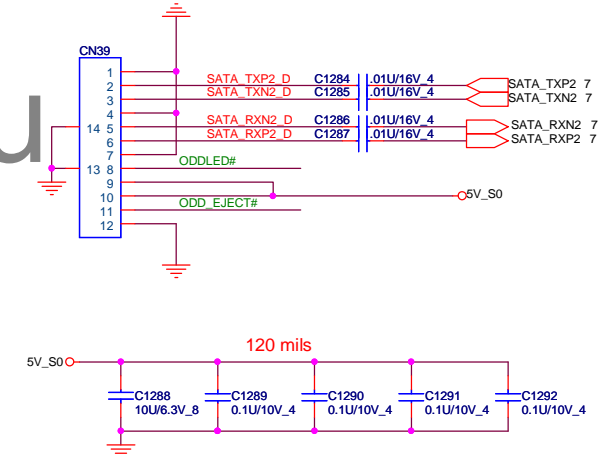


ODD BUTTON BTB CONN



B-01

SATA ODD CONN



Quanta Computer Inc.

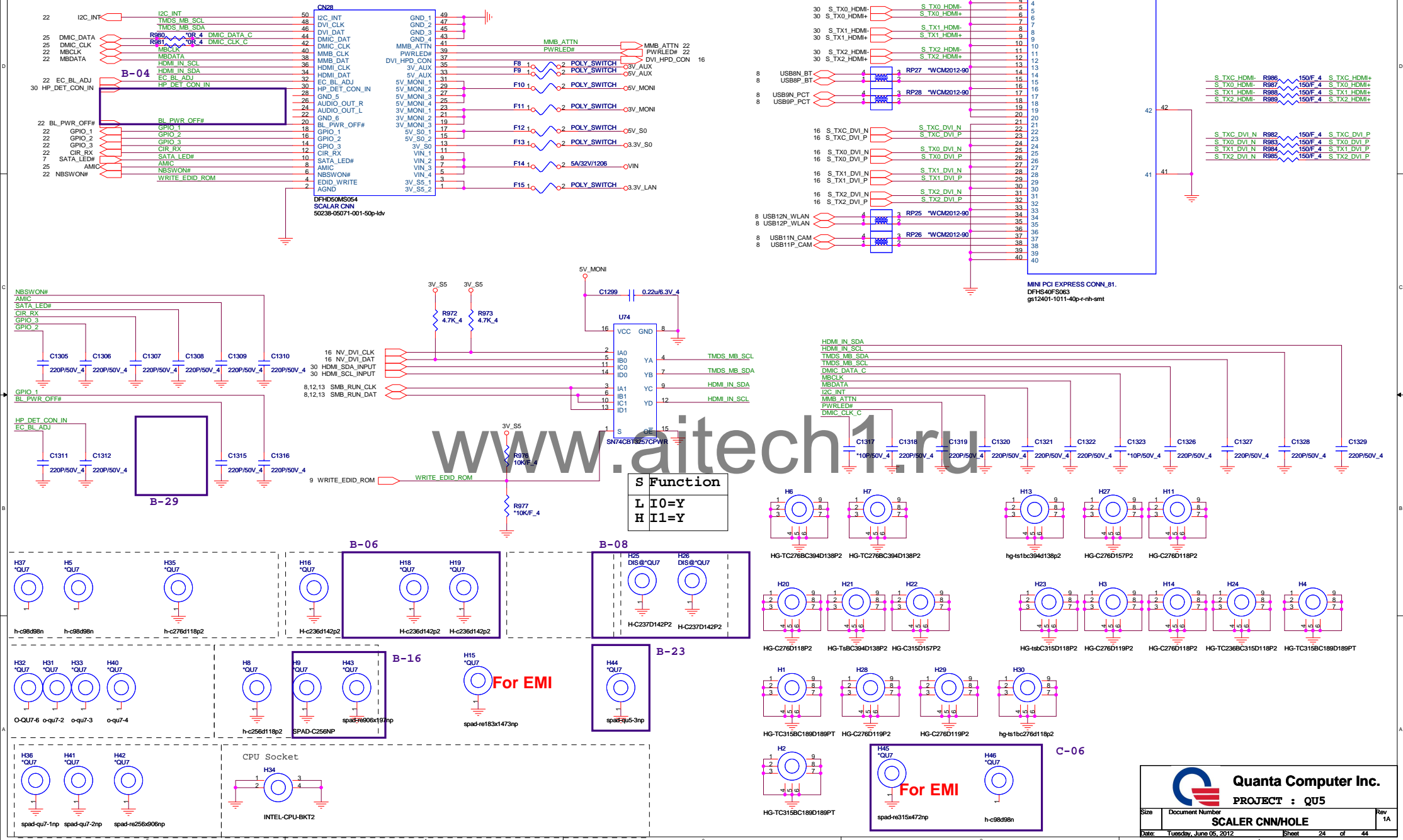
PROJECT : QU5

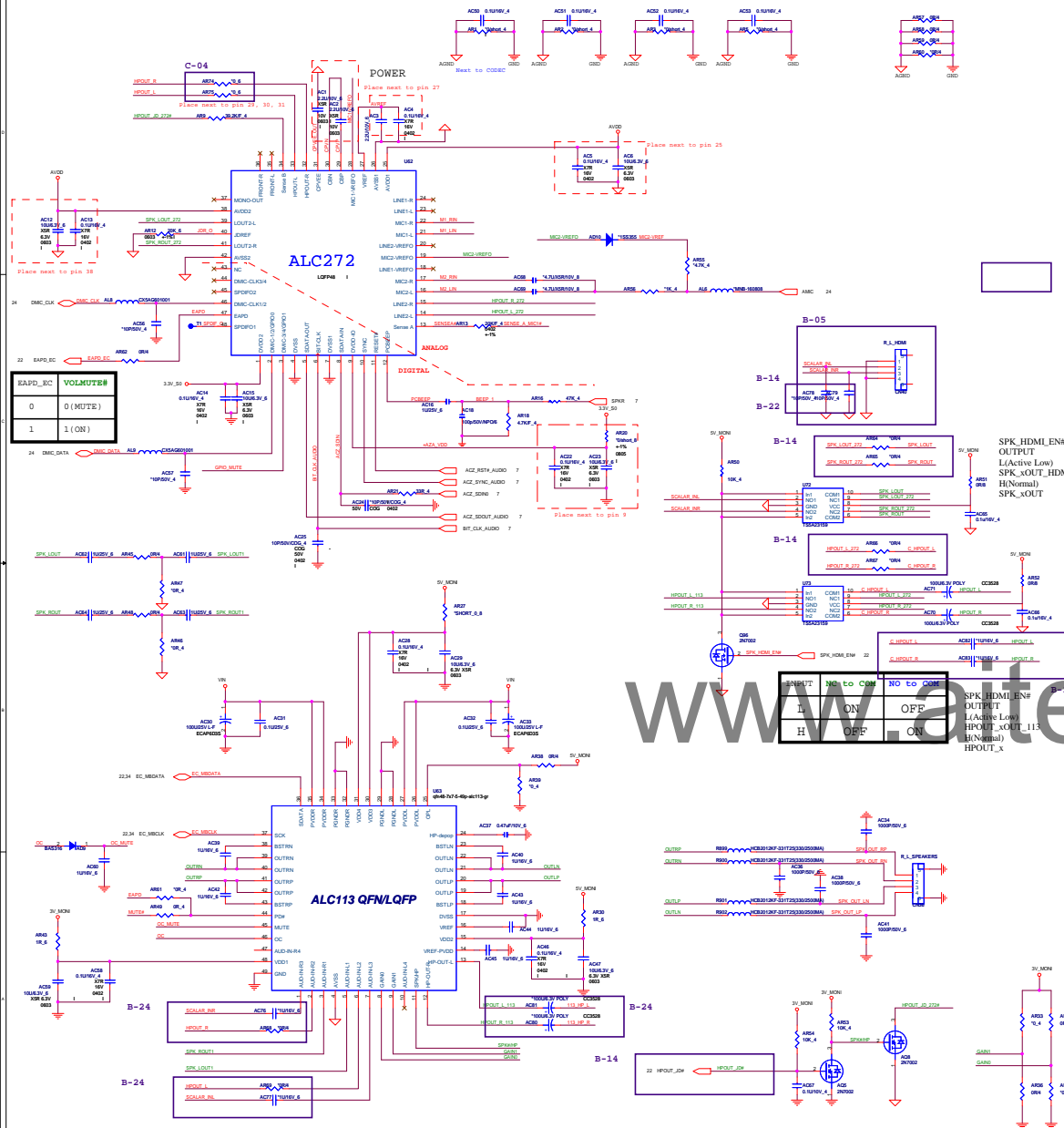
Size	Document Number	Rev
	HDD/ODD/FAN	1A

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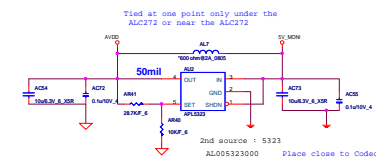
Scaler CNN

24

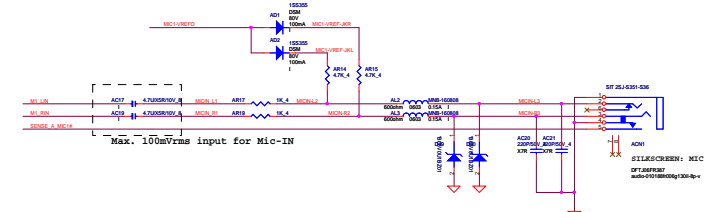




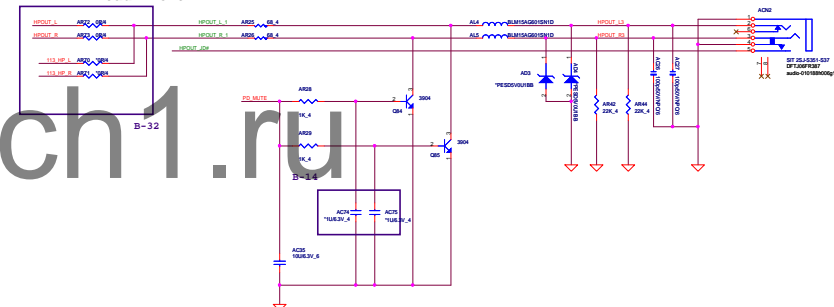
LDO



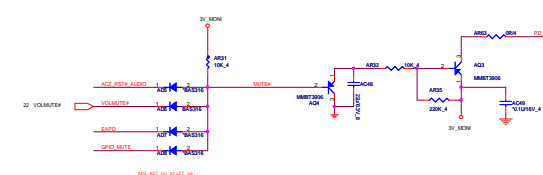
SYSTEM MIC



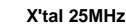
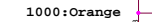
Head Phone



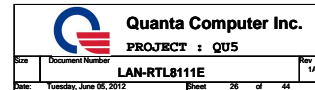
MUTE

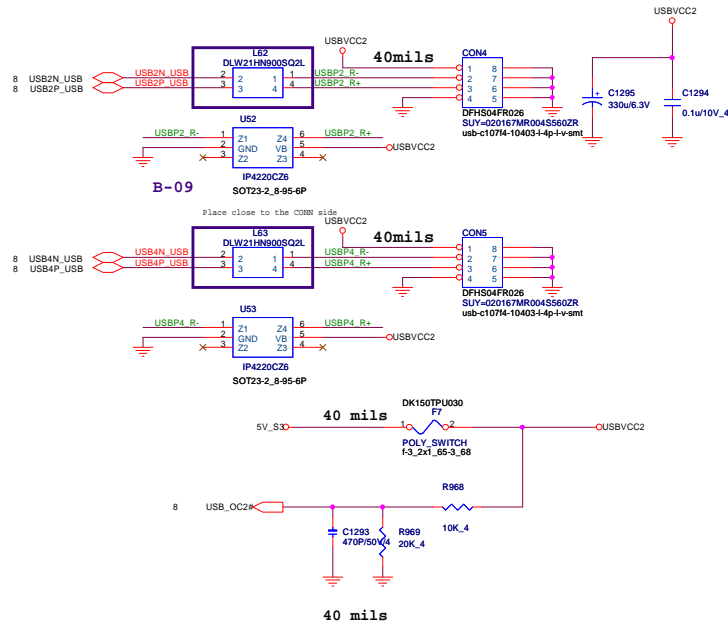


The diagram illustrates a transformer layout on a PCB. It features a central 'Transformer' block. To its left is the 'L' plane, which includes a 'GND' layer, a 'TX+' layer, a 'TX-' layer, another 'GND' layer, an 'RX+' layer, an 'RX-' layer, and a final 'GND' layer. To the right of the transformer is the 'R' plane, which includes a 'J' layer, an '4' layer, and a '5' layer. The entire layout is situated between a 'GND PLANE' at the bottom and an 'Isolated GND' at the top. The 'L' and 'R' labels are oriented vertically. The 'TX+' and 'TX-' labels are oriented horizontally. The 'RX+' and 'RX-' labels are oriented horizontally. The 'J', '4', and '5' labels are oriented vertically. The 'GND' and 'Isolated GND' labels are oriented horizontally. The 'Transformer' label is oriented horizontally. The 'GND PLANE' label is oriented horizontally. The 'Isolated GND' label is oriented horizontally.



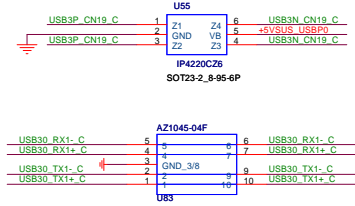
 always on
 always on
 always on
 blinking





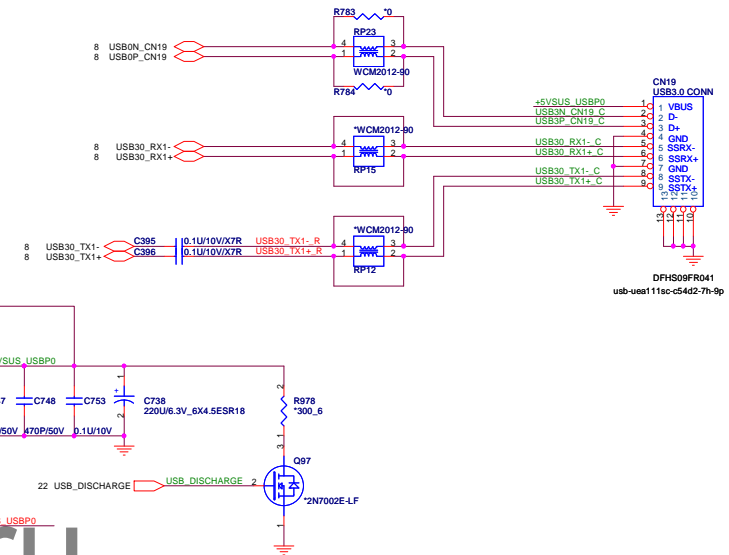
ESD Protection

layout note: close USB connector



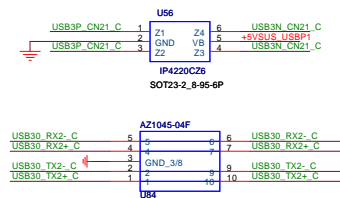
USB3.0/USB2.0 COMBO

USB 3.0



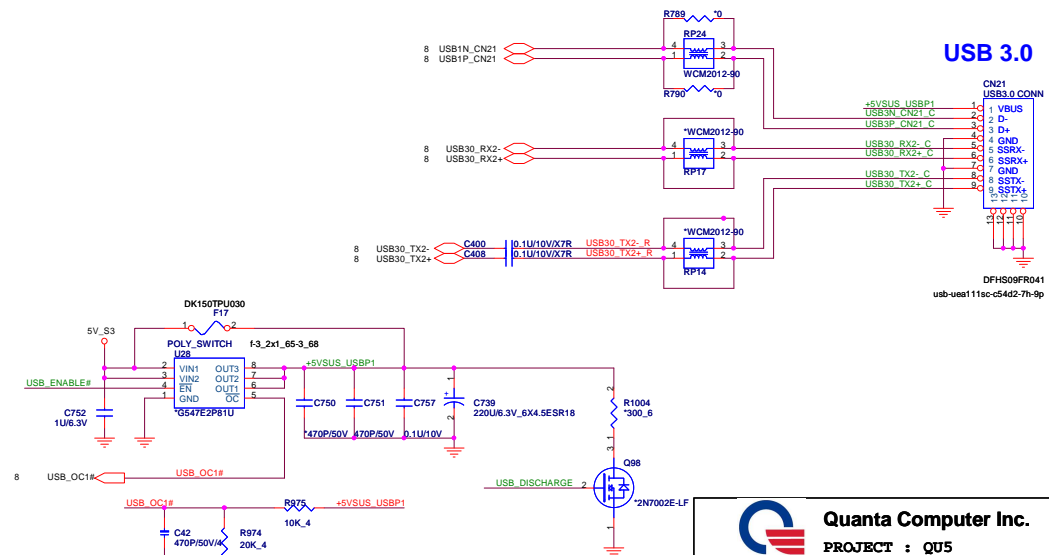
ESD Protection

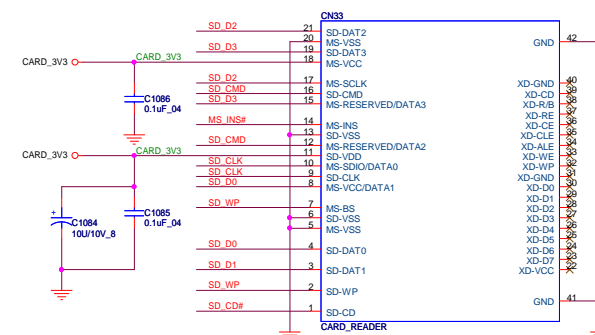
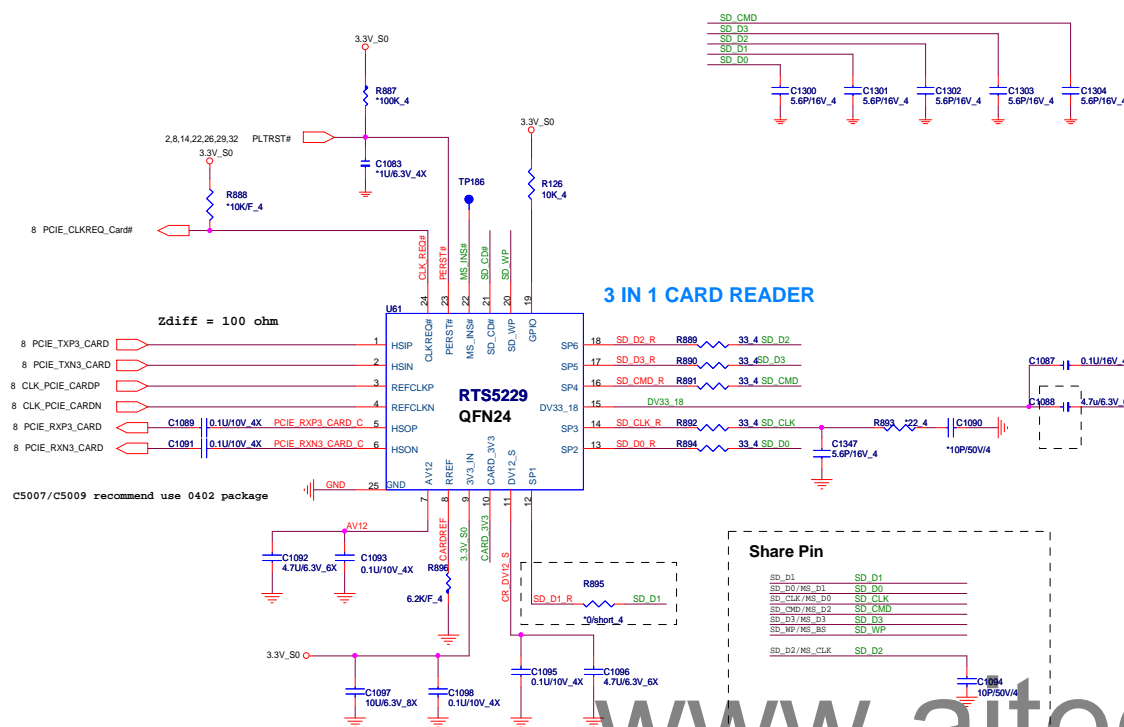
layout note: close USB connector



USB3.0/USB2.0 COMBO

USB 3.0



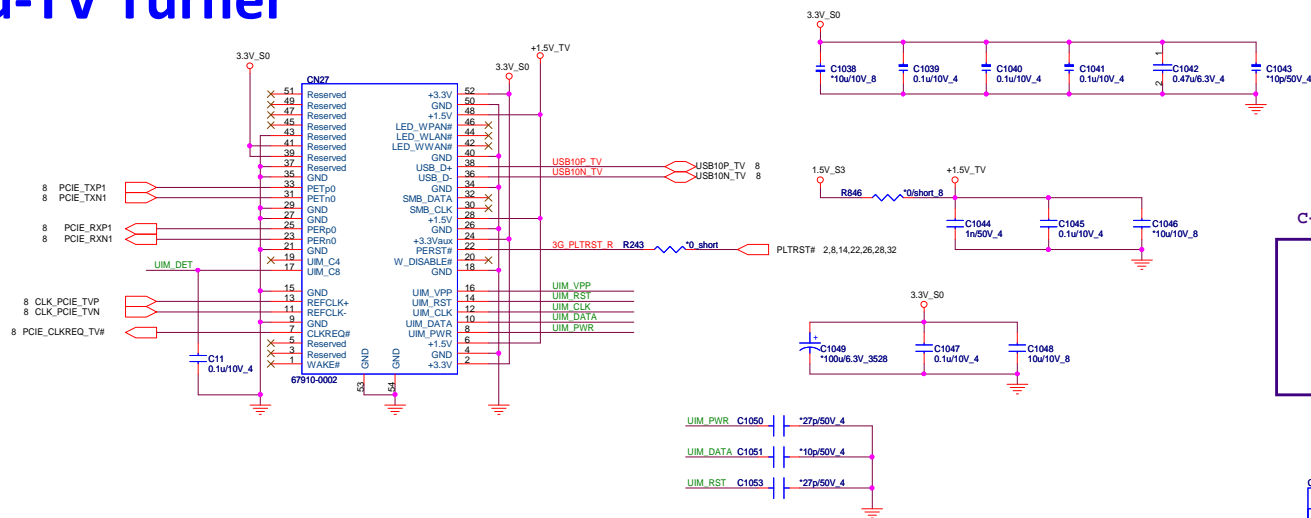


Share Pin

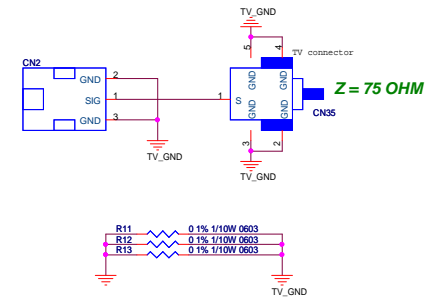
Share Pin	XD	MS	SD
SP1			SD_D1
SP2		MS_D1	SD_D0
SP3		MS_D0	SD_CLK
SP4		MS_D2	SD_CMD
SP5		MS_D3	SD_D3
SP6		MS_CLK	SD_D2
SP7		MS_B8	

LENOVO:
6 in 1 :SD, SDHC, SDXC, MMC, MS, MS-Pro
support SD3.0(SDR50/SDR104) or better

Mini Card-TV Turner

TV ANTENNA CONNECTOR
ANT. CONNECTOR

Del CN1, CN34, cancel Japan TV



C-01

Del *U54,*C1054,*C1052,*C25, cancel Japan TV

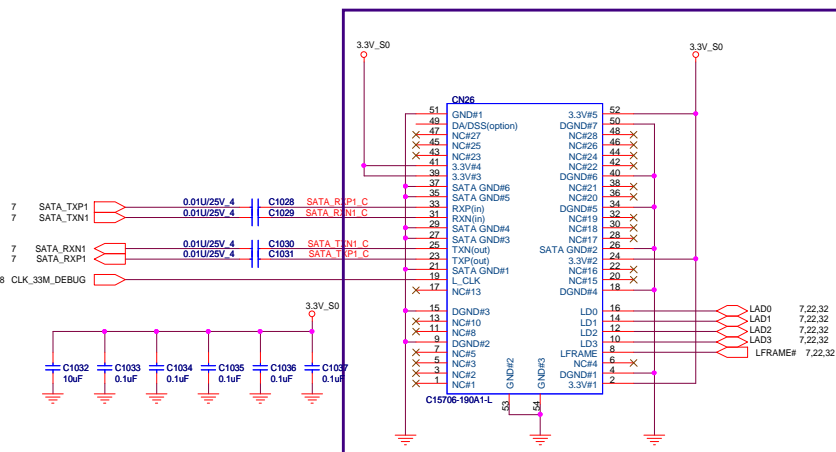
C-01

Del JSIM1,*R94, cancel Japan TV

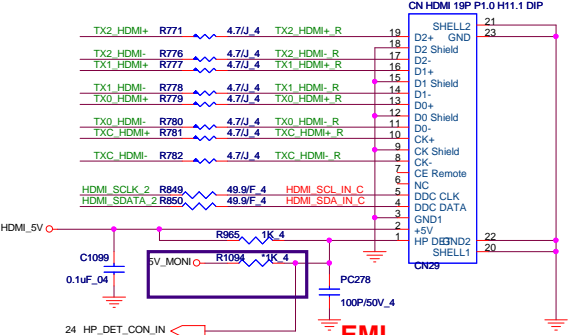
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Mini Card-mSATA

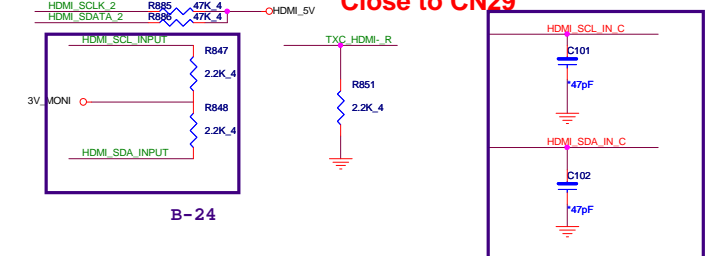
B-07



HDMI-INPUT PORT

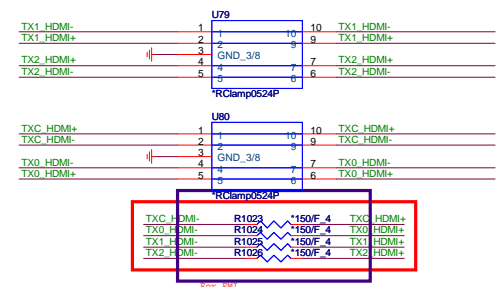


EMI
Close to CN29

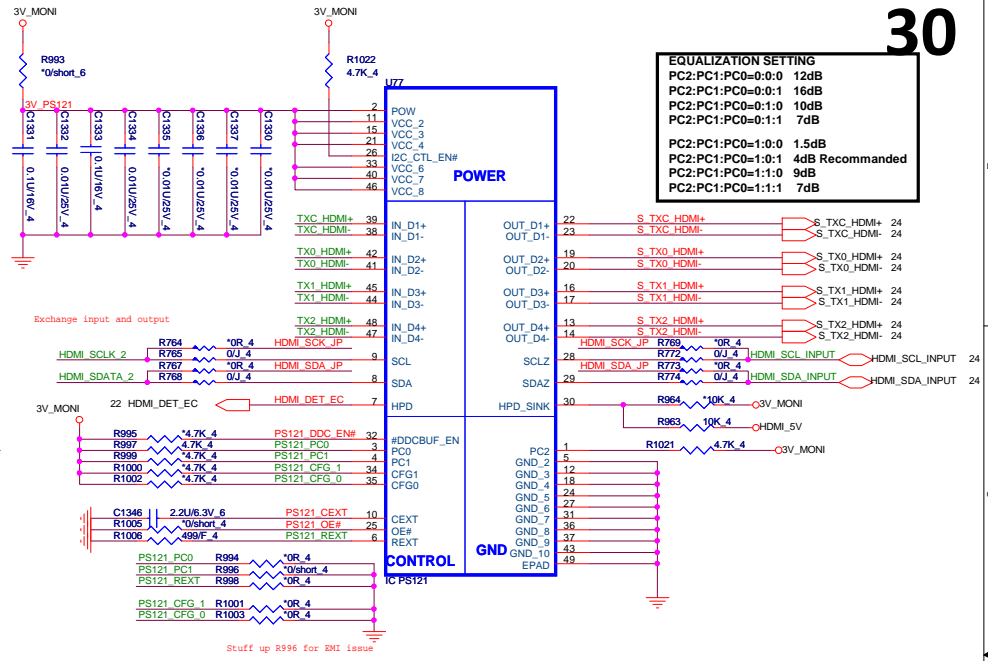
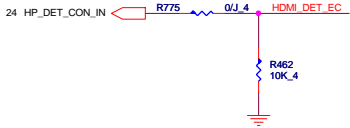


ESD Protection

layout note: close HDMI connector

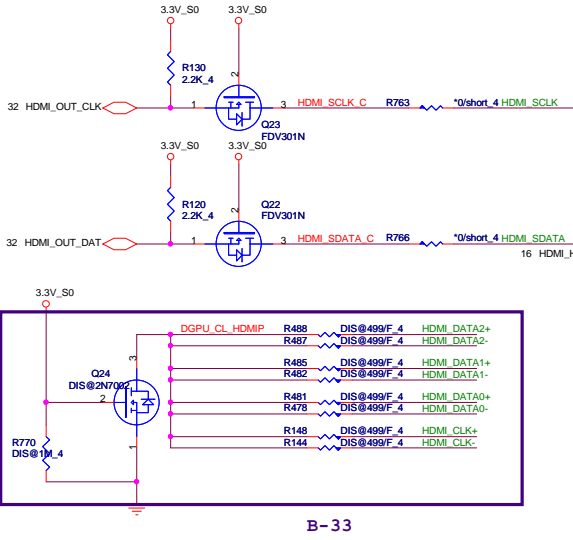


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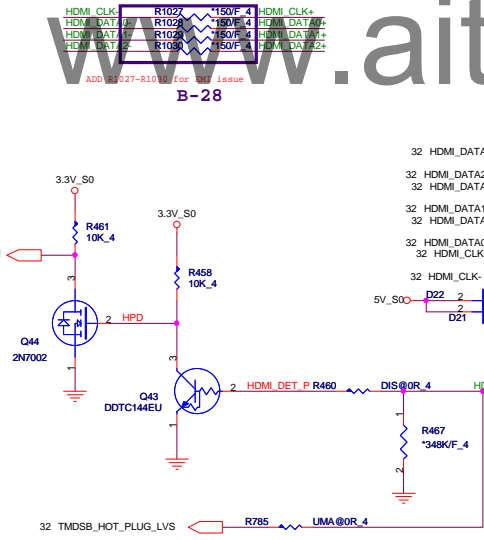


EQUALIZATION SETTING	
PC2:PC1:PC0=0:0:0	12dB
PC2:PC1:PC0=0:0:1	16dB
PC2:PC1:PC0=0:1:0	10dB
PC2:PC1:PC0=0:1:1	7dB
PC2:PC1:PC0=1:0:0	1.5dB
PC2:PC1:PC0=1:0:1	4dB Recommended
PC2:PC1:PC0=1:1:0	9dB
PC2:PC1:PC0=1:1:1	7dB

HDMI-OUT PORT

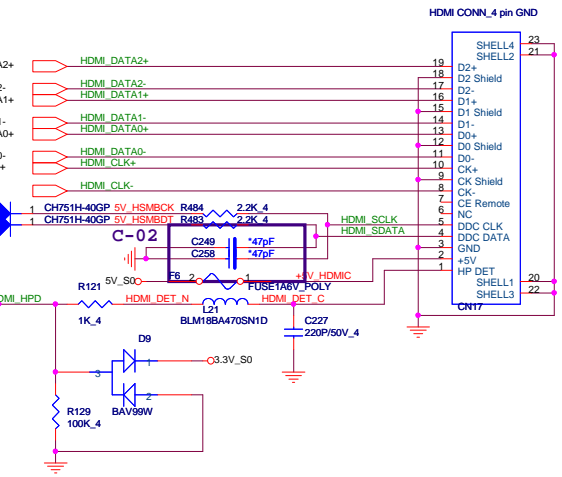
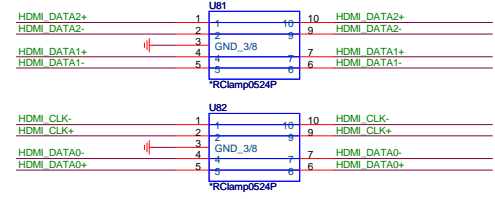


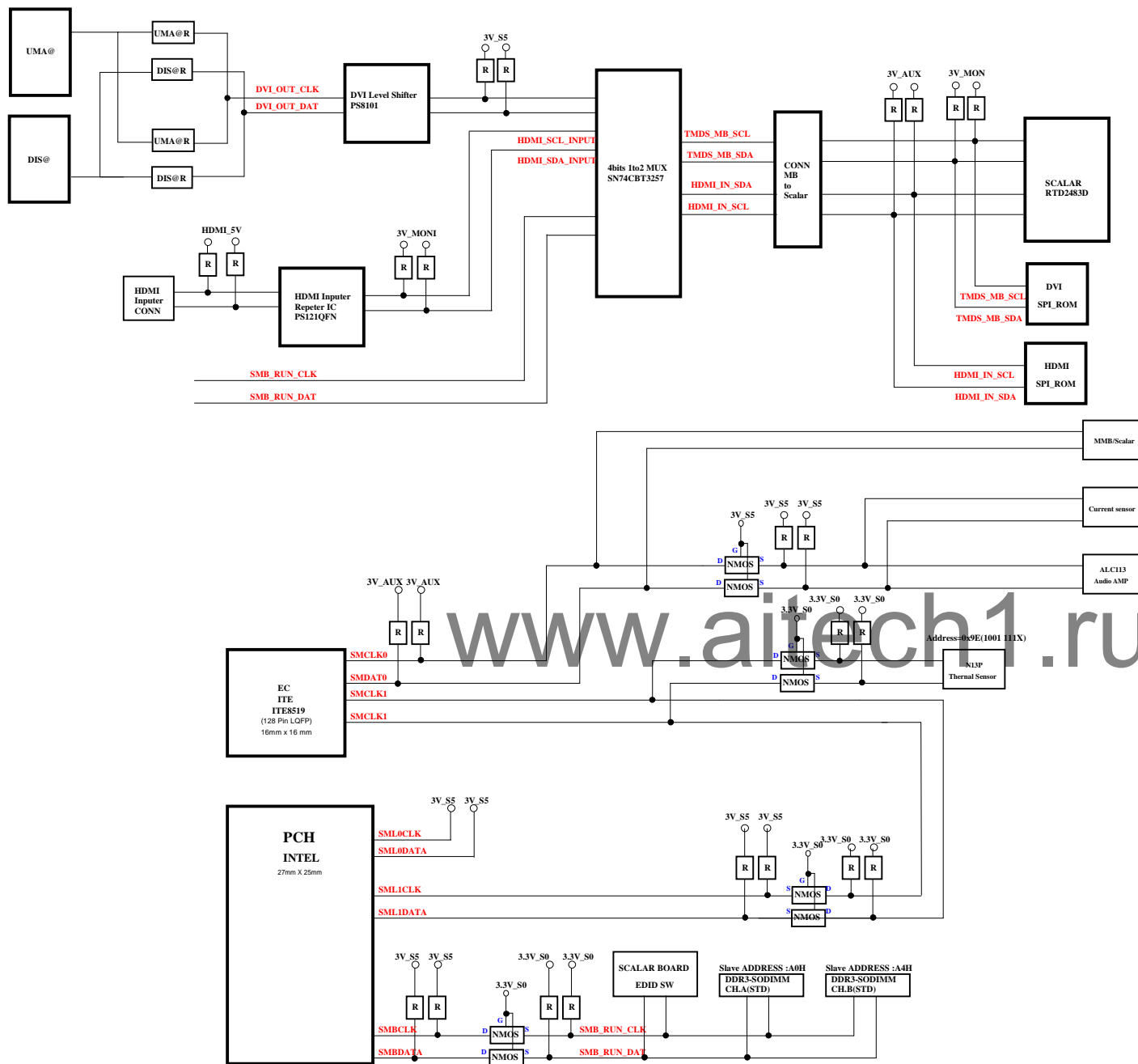
B-33



ESD Protection

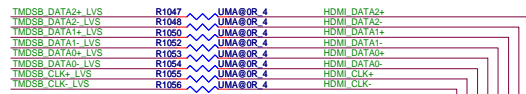
layout note: close HDMI connector





HDMI

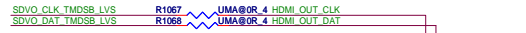
UMA



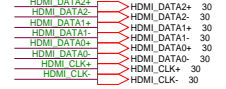
DIS



UMA



DIS



DVI

UMA



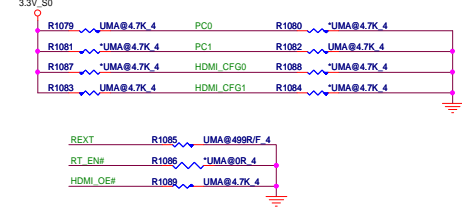
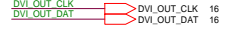
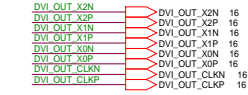
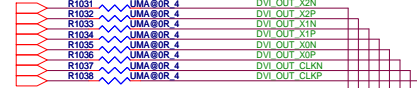
DIS



UMA

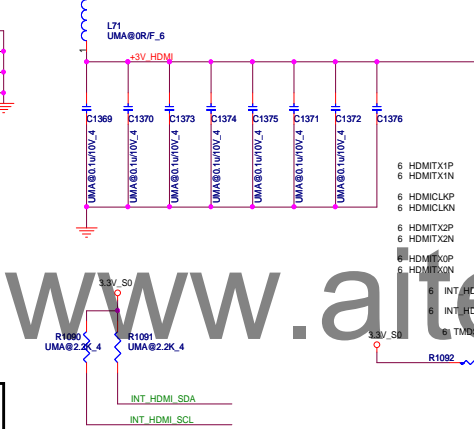


DIS



EQUALIZATION SETTING	
PC1:PC0=0:0	8dB
PC1:PC0=0:1	4dB Recommended
PC1:PC0=1:0	12dB
PC1:PC0=1:1	0dB

CFG = LOW: LOW-level input voltage: <0.40 V, LOW-level output voltage: 0.60 V
 CFG = HIGH: LOW-level input voltage: <0.44 V, LOW-level output voltage: 0.66 V
 HDMI_CFG1 = LOW: Passive DDC buffer
 HDMI_CFG1 = HIGH: Active DDC buffer



HDMI

UMA

DIS

UMA

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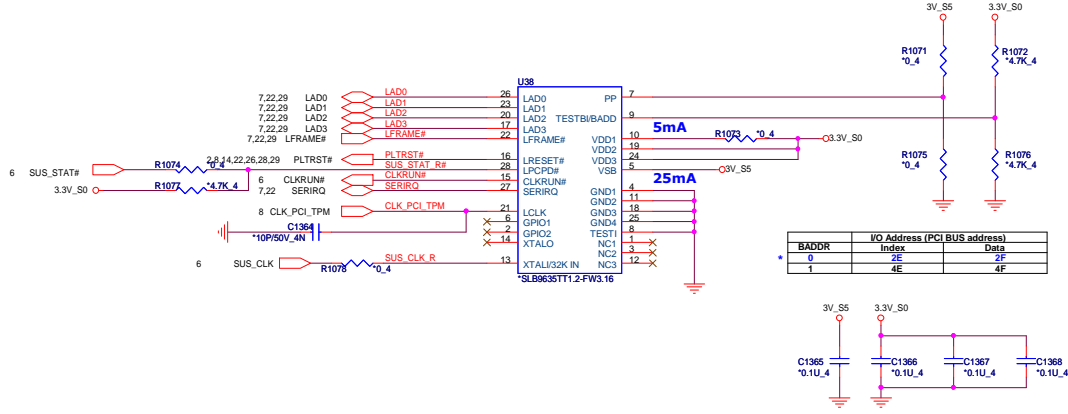
UMA

DIS

UMA

DIS

TPM

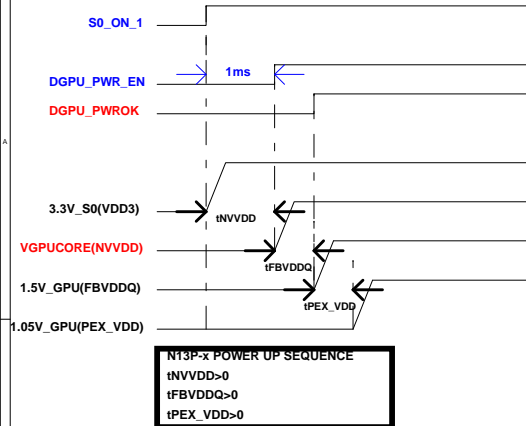


BADDR	Index	IO Address (PCI BUS address)	Data
0	2E	2F	2F
1	4E	4F	4F



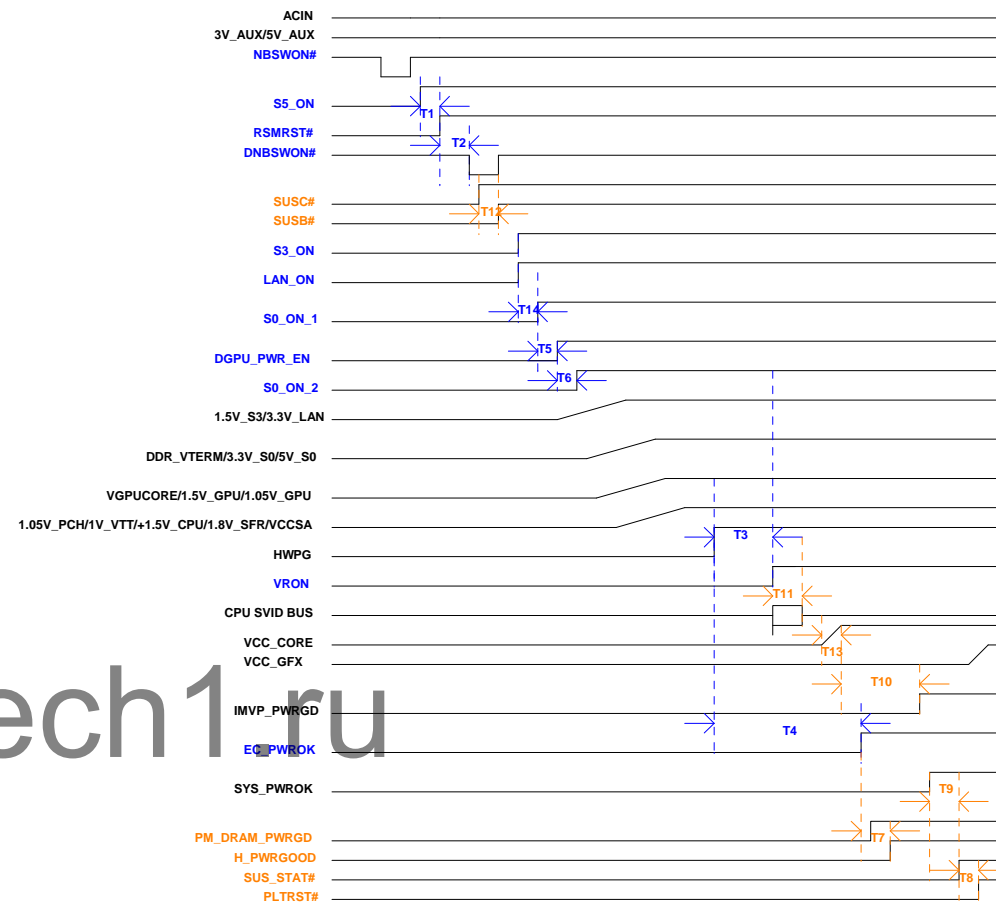
Quanta Computer Inc.
 PROJECT : Q05

N13P-x POWER UP SEQUENCE



QU7 POWER-ON SEQUENCE

32



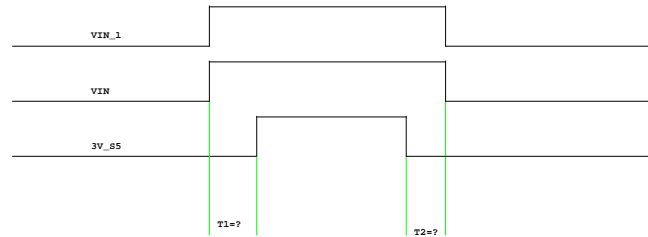
System Power Sequence
 T1: S5_ON TO RSMRST# = 30ms (spec:mini 10ms)
 T2: RSMRST# TO DNBSWON# = 110ms (spec:mini 100ms)
 T3: HWPG TO VRON = 10ms
 T4: HWPG TO EC_PWROK = 99ms (Min)
 T5: S0_ON_1 TO DGPU_PWR_EN = 2.1 ms
 T6: DGPU_PWR_EN TO S0_ON_2 = 3.2 ms
 T7: EC_PWROK TO H_PWRGOOD = 2ms(Min)
 T8: SUS_STAT# TO PLTRST# = 60us(Min)
 T9: SYS_PWROK TO SUS_STAT# = 1ms(Min)
 T10: VCC_CORE TO IMVP_PWRGD = 5ms(Max)
 T11: VRON to accept SVID command = 5ms(Max)
 T12: SUSC# to SUSB# = 30us(Min)
 T13: VCC_CORE ramp time = 50-2000us
 T14: LAN_ON(S3_ON) TO S0_ON_1 = 1ms

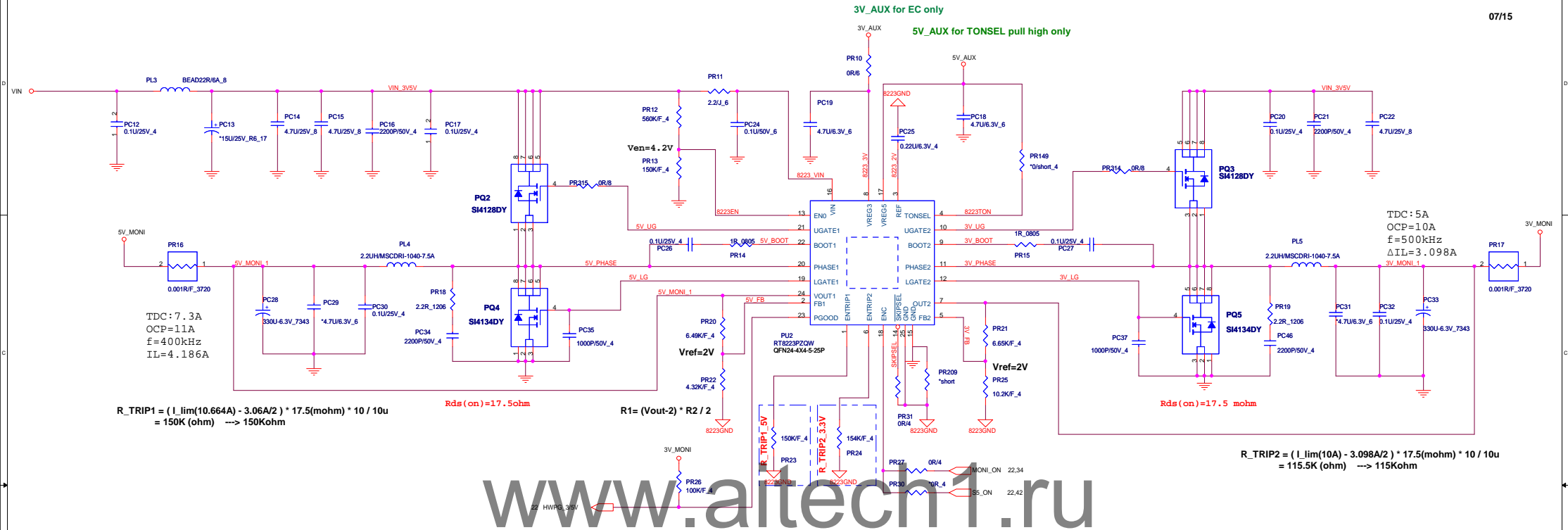
Voltage Rails

Power	Voltage	S0	S3	S4	S5	G3	Ctl Signal	Location
+3V_RTC	3V	ON	ON	ON	ON	ON		Mother board
VIN	19.5V	ON	ON	ON	ON	OFF	Adaptor in	Mother board
5V_AUX	5V	ON	ON	ON	ON	OFF	Adaptor in	Mother board
3V_AUX	3.3V	ON	ON	ON	ON	OFF	Adaptor in	Mother board
12V_AUX	12V	ON	ON	ON	ON	OFF	Adaptor in	Mother board
5V_S5	5V	ON	ON	OFF	OFF	OFF	S5_ON	Mother board
3V_S5	3V	ON	ON	OFF	OFF	OFF	S5_ON	Mother board
1.2V_S5	1.2V	ON	ON	OFF	OFF	OFF	S5_ON	Mother board
1.5V_S3	1.5V	ON	ON	OFF	OFF	OFF	S3_ON	Mother board
3.3V_LAN	3V	ON	Note	Note	Note	OFF	LAN_ON	Mother board
5V_S0	5V	ON	OFF	OFF	OFF	OFF	S0_ON_1	Mother board
3.3V_S0	3V	ON	OFF	OFF	OFF	OFF	S0_ON_1	Mother board
DDR_VTERM	0.75V	ON	OFF	OFF	OFF	OFF	S0_ON_1	Mother board
1.05V_PCH	1.05V	ON	OFF	OFF	OFF	OFF	S0_ON_2	Mother board
1V_VTT	1V	ON	OFF	OFF	OFF	OFF	S0_ON_2	Mother board
VCCSA	By VID	ON	OFF	OFF	OFF	OFF	HWPG_VTT	Mother board
+1.5V_CPU	1.5V	ON	OFF	OFF	OFF	OFF	S0_ON_2	Mother board
1.8V_SFR	1.8V	ON	OFF	OFF	OFF	OFF	S0_ON_2	Mother board
VGPUCORE	By VID	ON	OFF	OFF	OFF	OFF	DGPU_PWR_EN	Mother board
1.5V_GPU	1.5V	ON	OFF	OFF	OFF	OFF	DGPU_PWROK	Mother board
1.05V_GPU	1.05V	ON	OFF	OFF	OFF	OFF	DGPU_PWROK	Mother board
VCC_CORE	By VID	ON	OFF	OFF	OFF	OFF	VRON	Mother board

Note: Depend on WOL

```
ramp-up time for all power rails
50 us <All power rails except 5V_S5 <40 ms
100 us <5V_S5<40 ms
```





$$I_{ripple} = (V_{in} - V_{out}) * V_{out} / (V_{in} * L * f)$$

O.C.P setup information

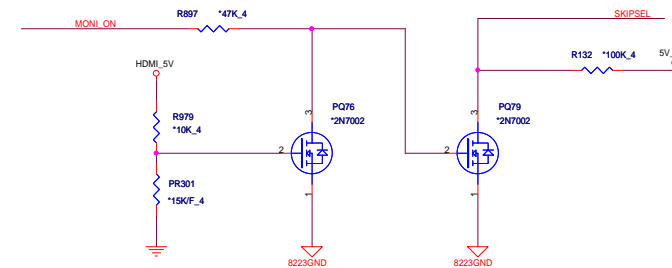
Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
5V	17.5m_Max	14.25	4.186	400	2.2uH	150K
3.3V	17.5m_Max	10	3.098	500	2.2uH	115K

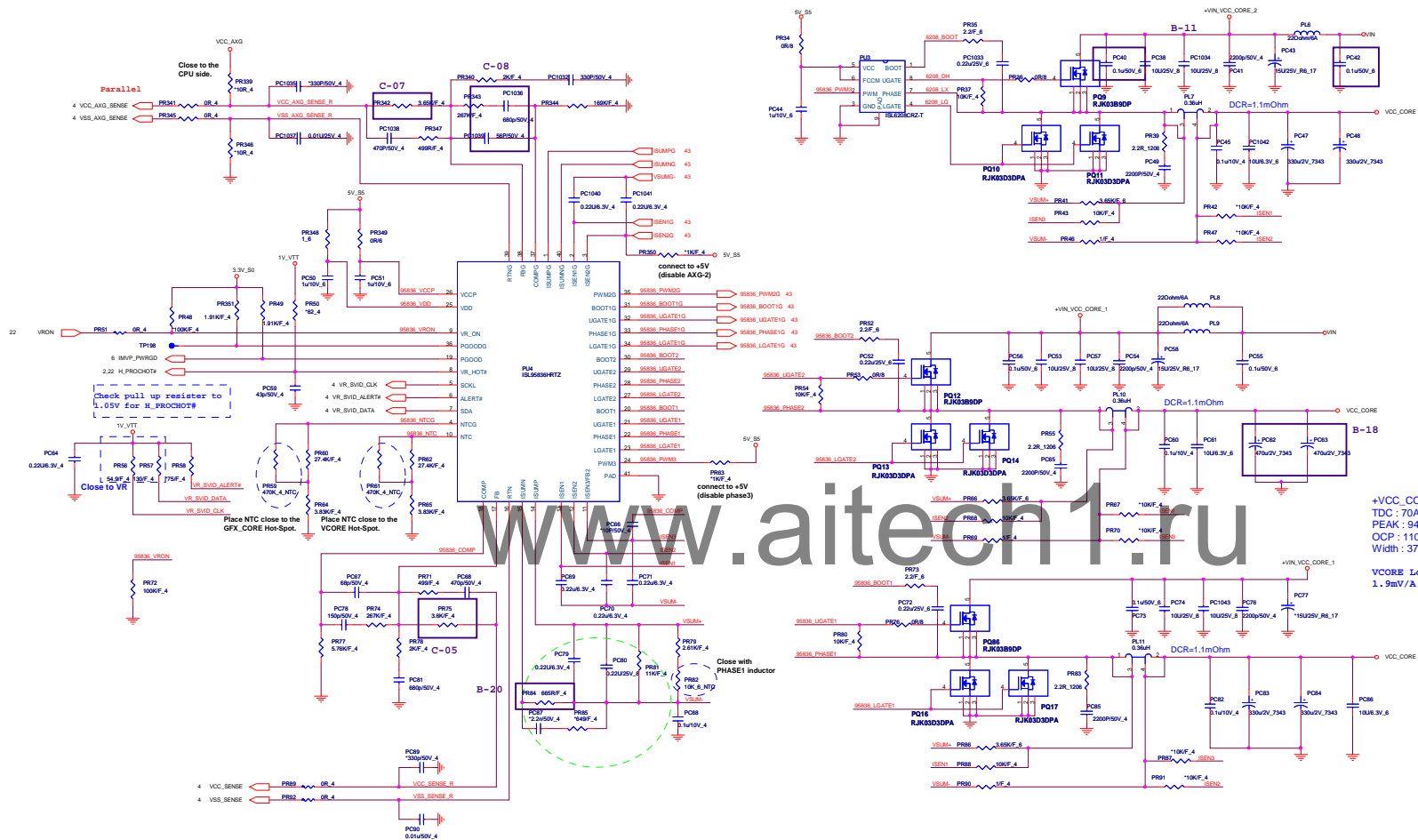
L/S Mosfet parameter

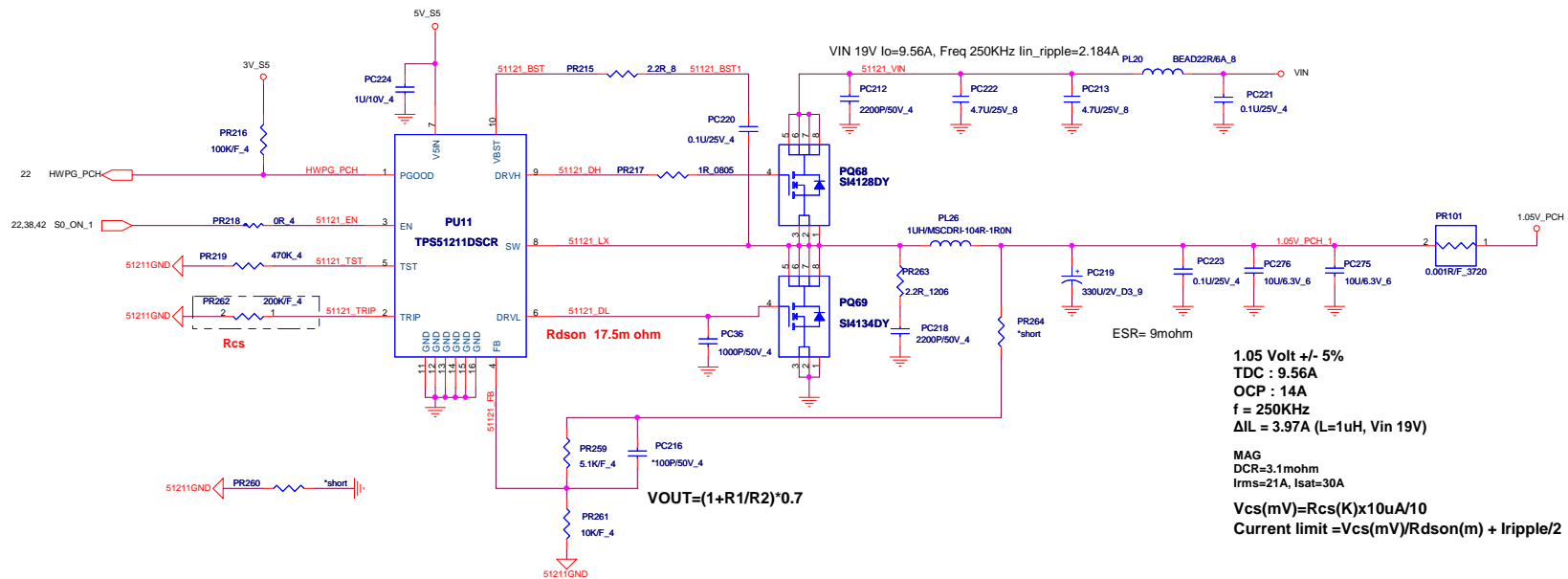
Mosfet	Package	ID (Ta=25C)	Rds_on_max
Si4134DY	SO-8	9.9A/14A	17.5m
AO4712	SO-8	10A/11.2A	18.0m
AO4710	SO-8	11A/12.7A	14.2m
AP4438GSM	SO-8	7A/11.7A	18.0m
DMG4812	SO-8	9.6A/10.7A	18.5m
AON7702	DFN3x3	11A/20A	14.0m

Power On sequencing

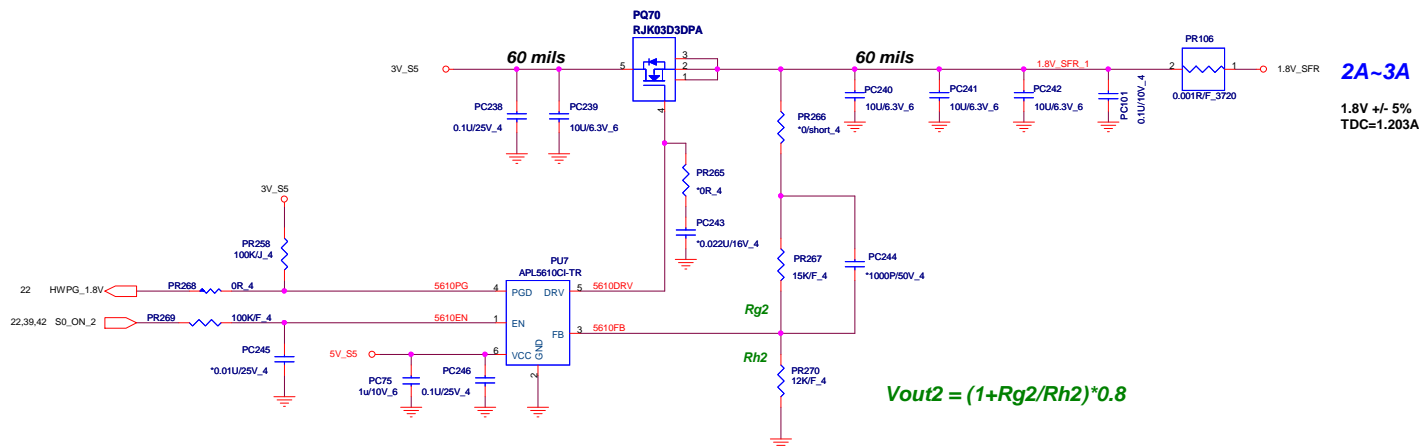
EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON



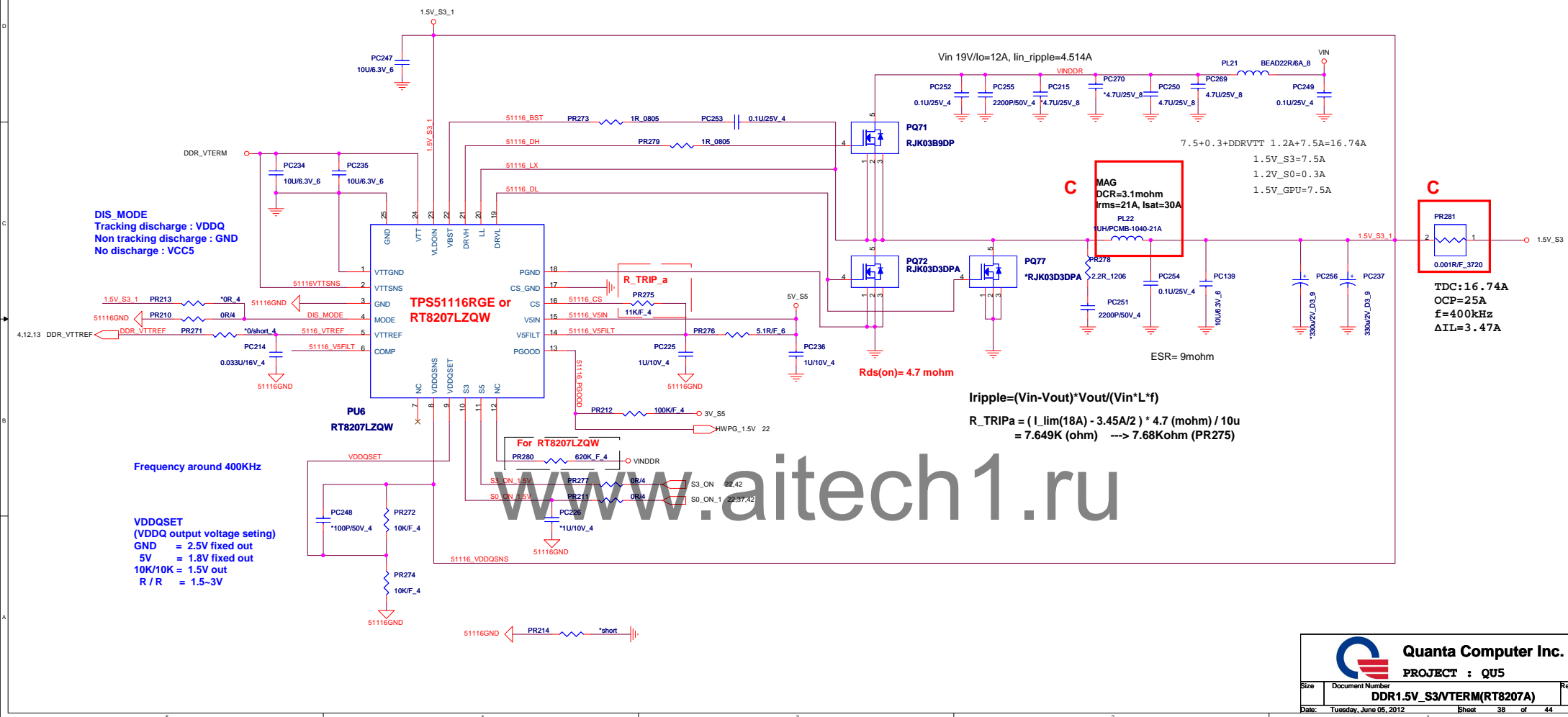


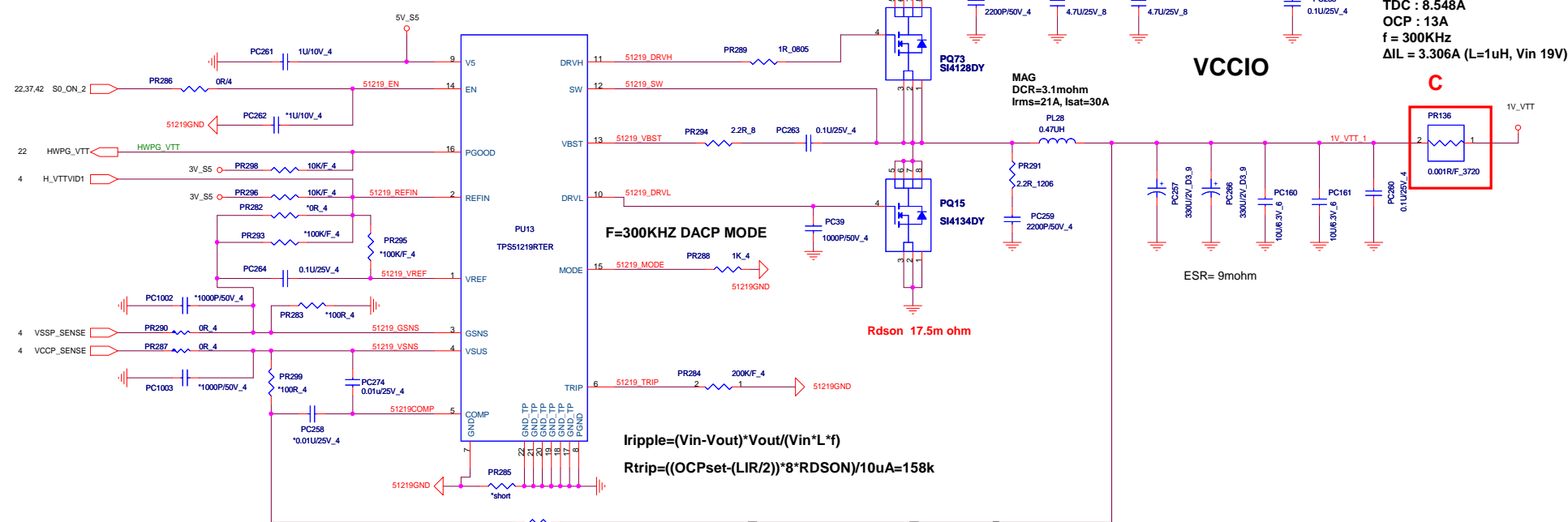


1.8V_SFR



DDR3 1.5V_S3 (TPS51116RGE or RT8207LZQW)



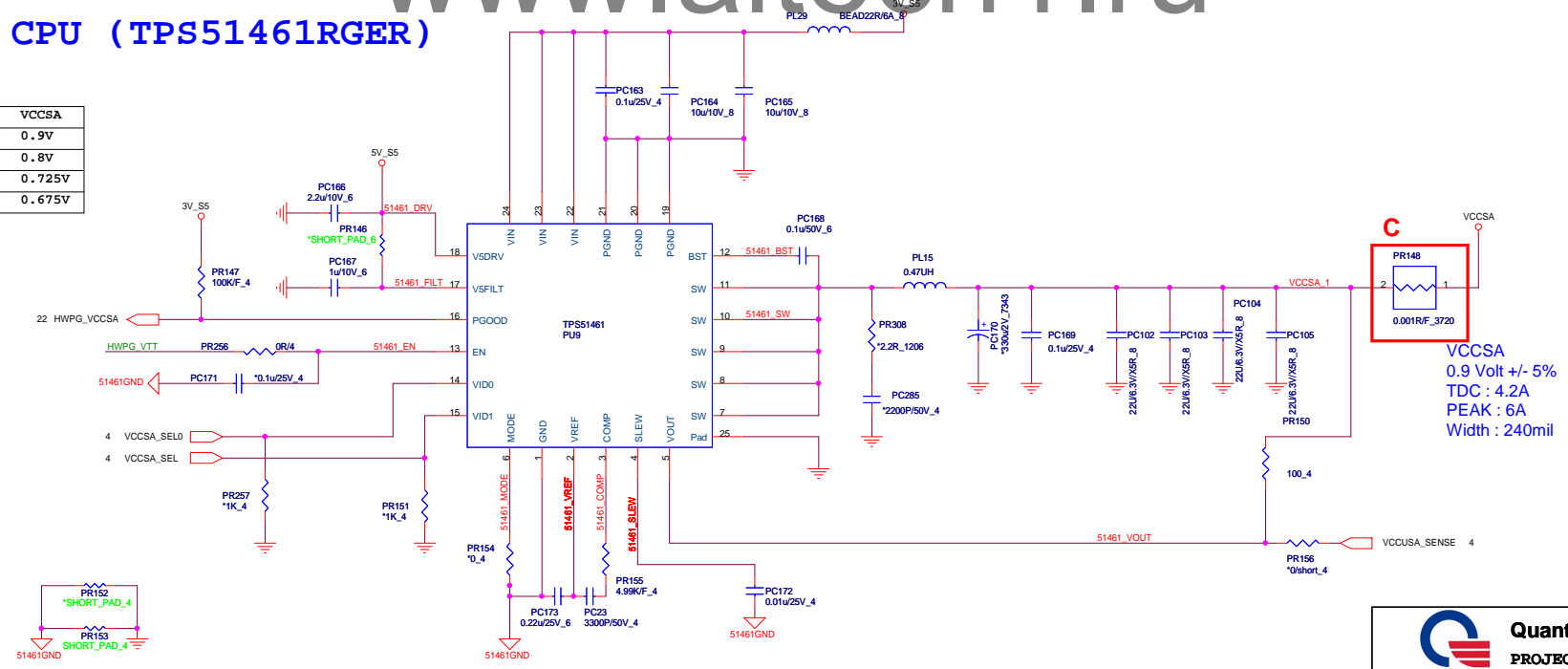


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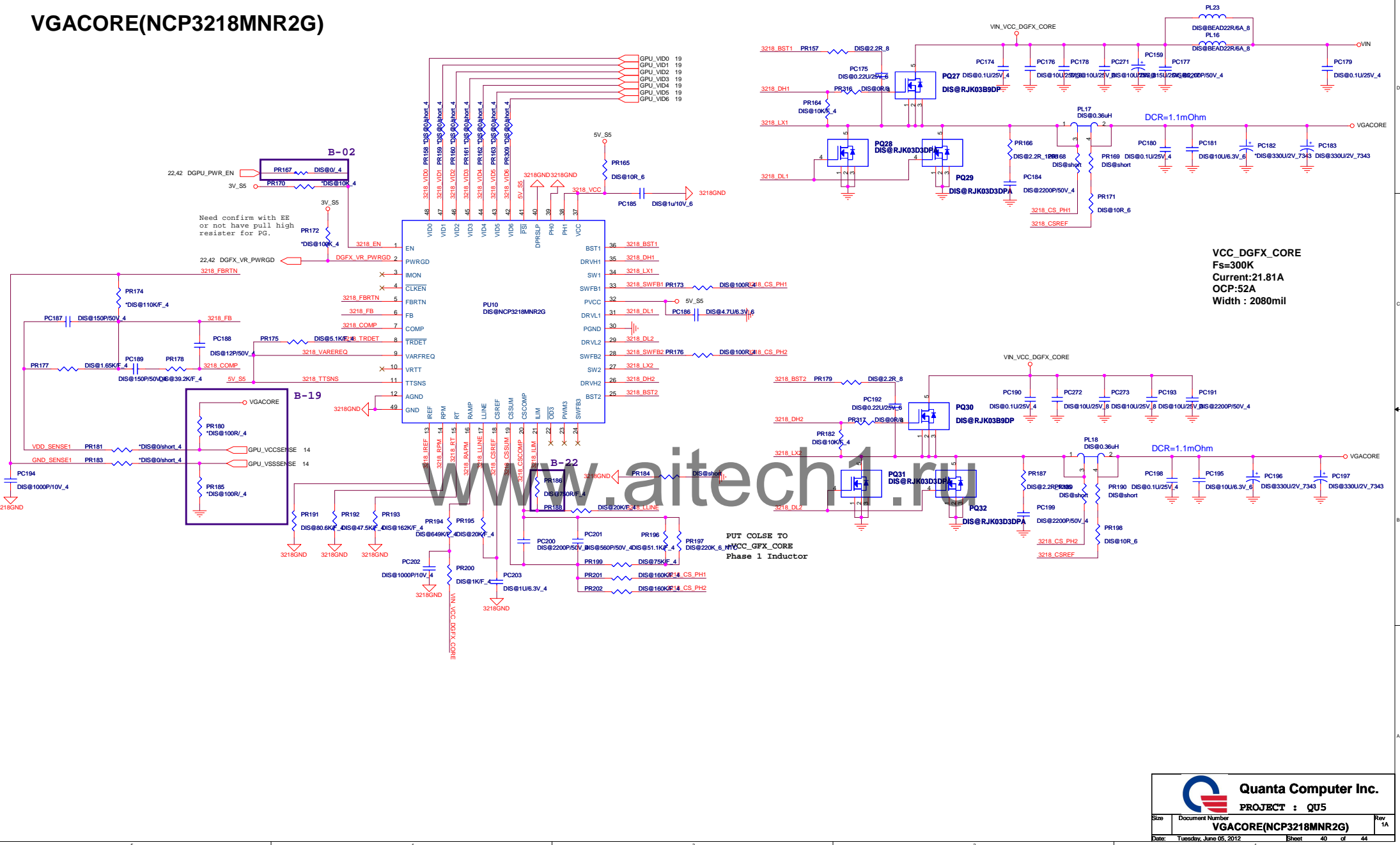
VID0	VID1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

VCCSA_SEL	VCCSA
1	0.8V
0	0.9V

default 0.9V



VGACORE(NCP3218MNR2G)



Quanta Computer Inc.

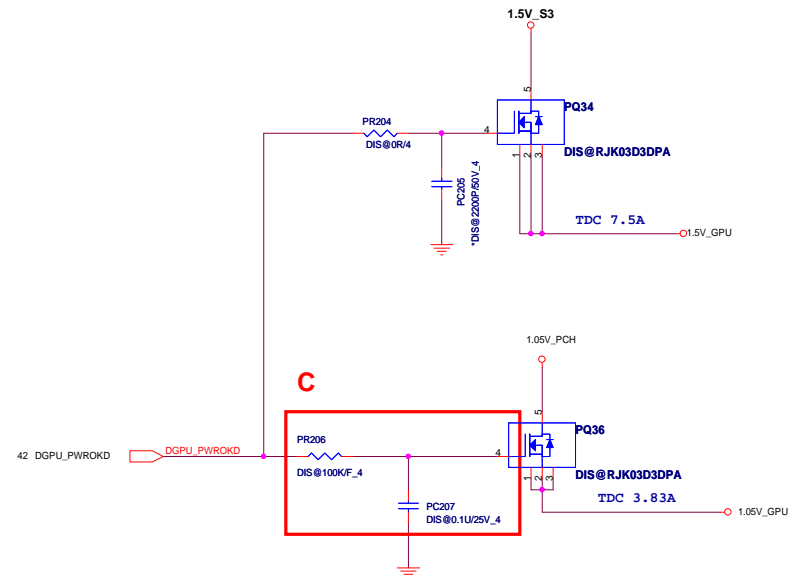
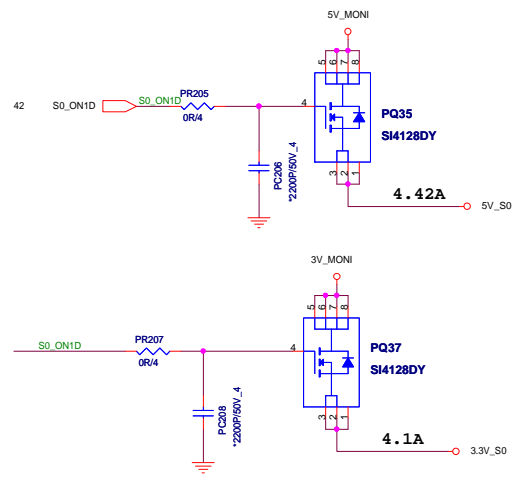
PROJECT : QU5

Size	Document Number	Rev
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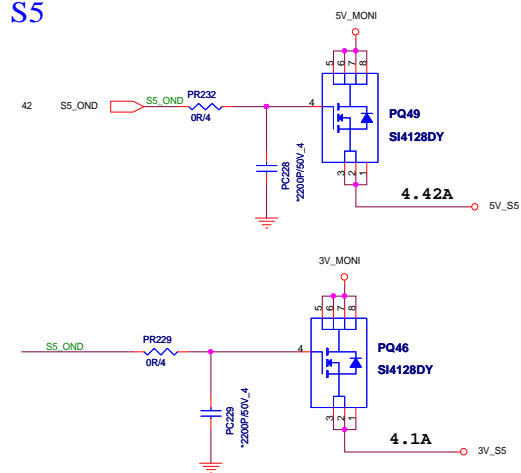
Date: Tuesday, June 05, 2012 Sheet 40 of 44

VGA

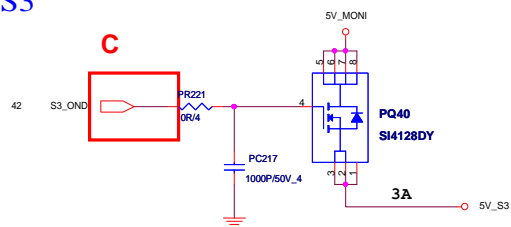
S0



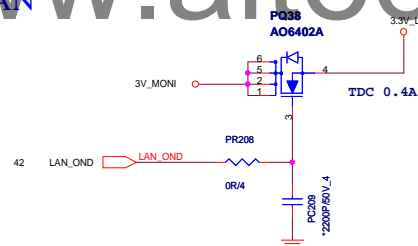
S5



S3

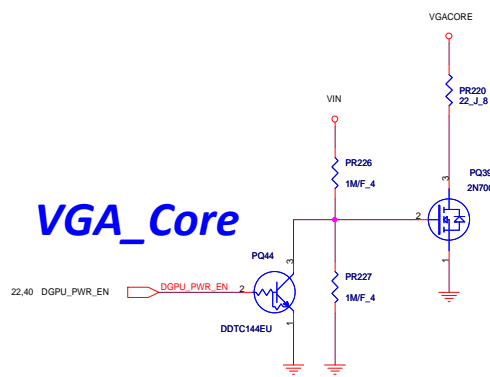


LAN

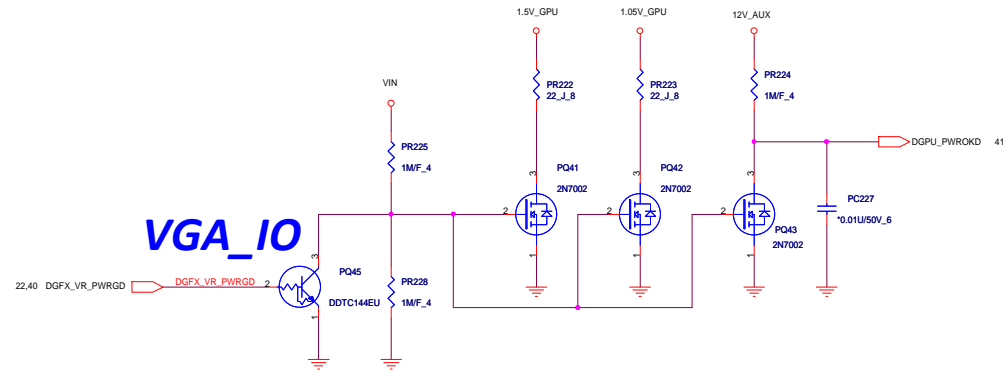


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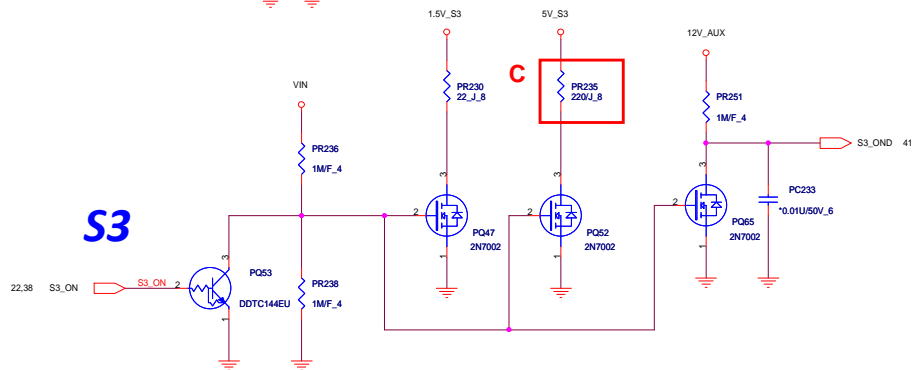
VGA_Core



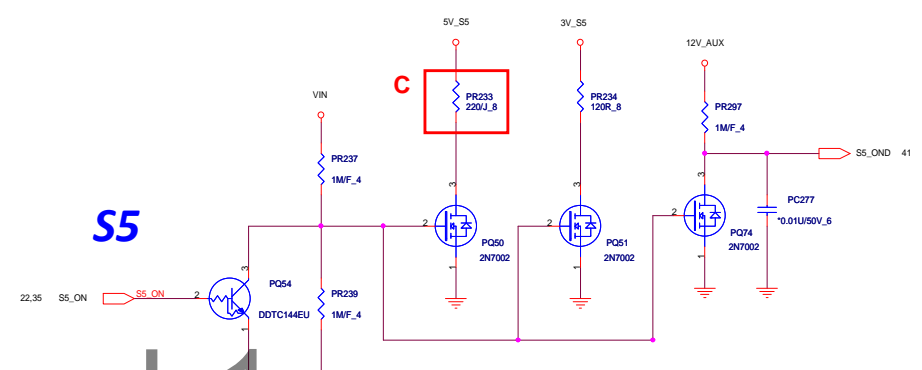
VGA_IO



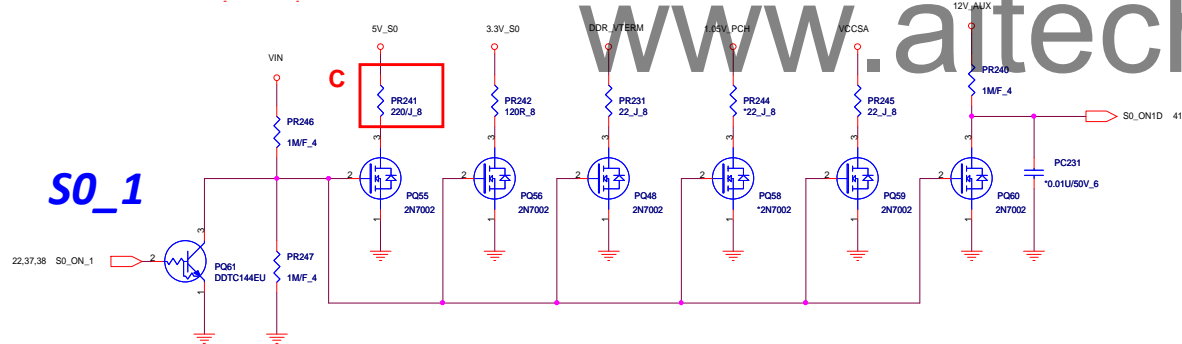
S3



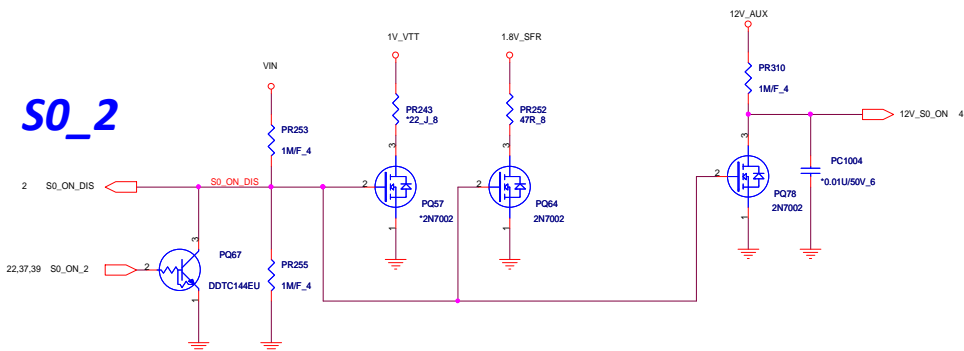
S5



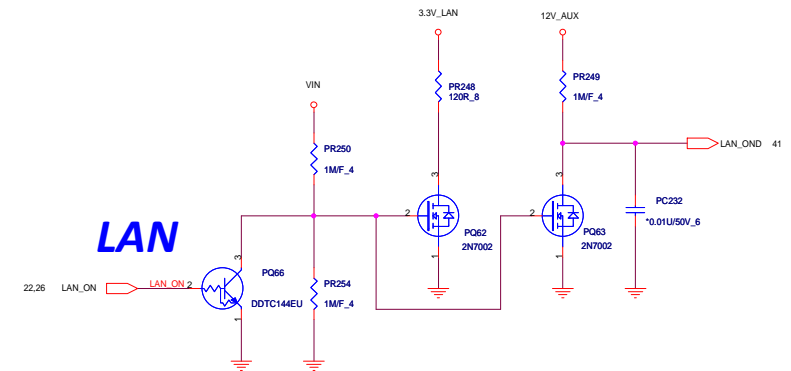
S0_1



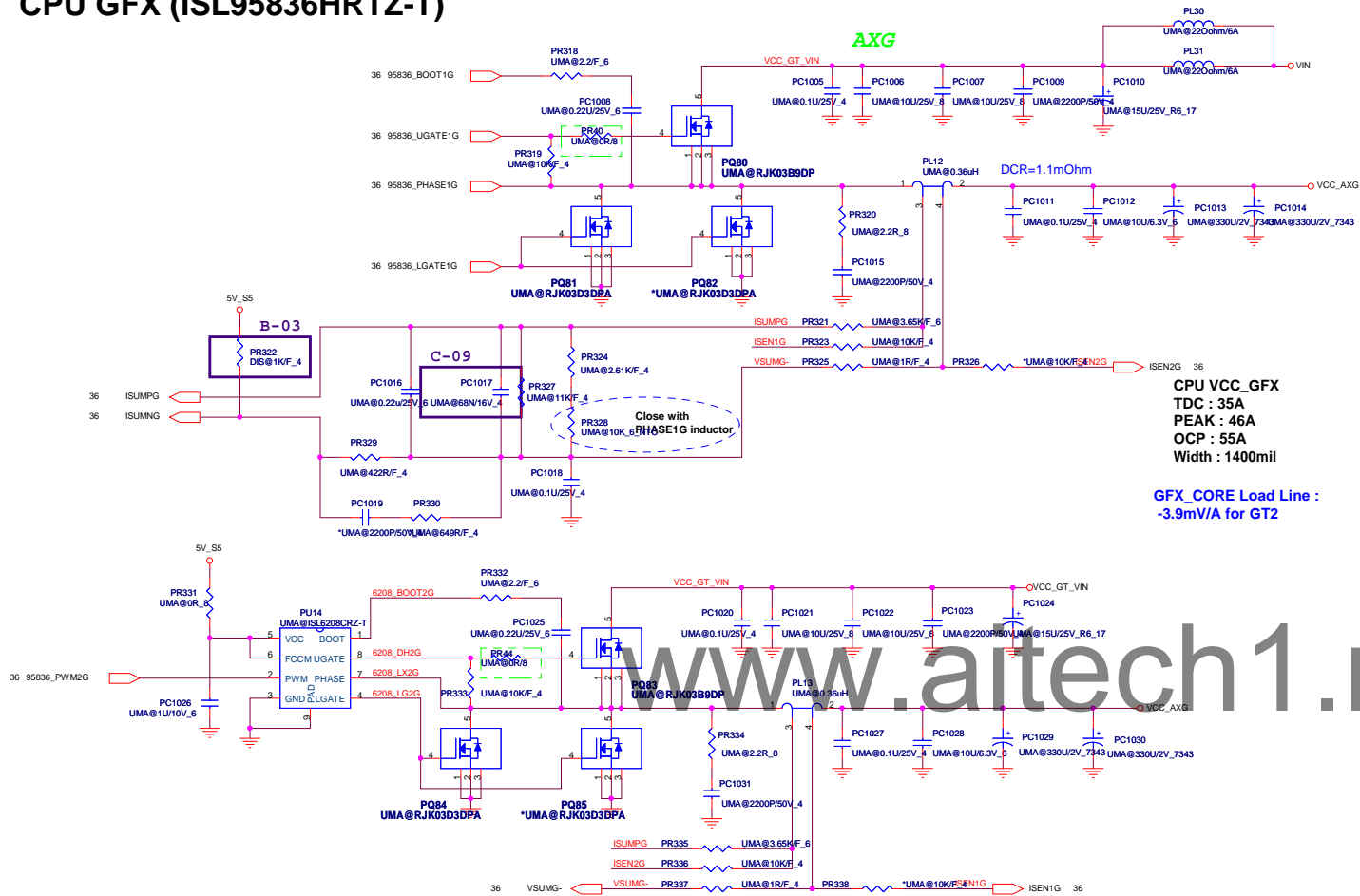
S0_2



LAN



CPU GFX (ISL95836HRTZ-T)



QU5 Mother Board Schematics Revision History

PCB Rev	Sch Rev	BOM Rev	DATE	Change List & Description
A	01	-	02/29/12'	1st Release
B	02	-	03/29/12'	A - B B-01 : Delete CON6, R960. QU5 don't support ODD BTB function - P23 B-02 : Stuff PR167 0ohm for VGA Core power enable (DIS SKU ONLY) - P40 B-03 : Stuff PR322 1Kohm for CPU core no output (DIS SKU ONLY) - P43 B-04 : Cancel CN28 pin22(GND), 24(SCALAR_INR), 26(SCALAR_INL), 28(GND) path to U72 for HDMI audio noise issue, Delete R1093, R1094, R1095, C1100 - P24 B-05 : Add CN40, C1101 for HDMI audio noise issue- P25 B-06 : H17 change NUT H=6.5 from BOM, Add H18 NUT H=2.8 from BOM - P24 B-07 : Change MiniPCIe Connector to H=9 from H=4 for BOM - P29 B-08 : Delete H25, H26 for UMA SKU - P24 B-09 : L62, L63 stuff on UMA SKU for BOM - P27 B-10 : Delete C1358, C1359, C1362, C1363, C1356, C1357, C1360, C1361 on DIS SKU for BOM - P06 B-11 : PC40, PC42 use 1uF 0402 component change to 1uF 0603 for BOM change - P36 B-12 : VR43 change to 15Kohm from 10Kohm for HWID incorrect - P19 B-13 : VR130 stuff 0ohm for can't display issue on UMA SKU- P16 B-14 : - P25 AC78 & AC79 AR64& AR65 For remove. B-15 : - P16 Dummy to C1027 for DIS SKU. B-16 : - P24 Add footprint : spad-re906x197np B-17 : - P16 Add R1097 & R1096 for co-lay P88171. B-18 : - P36 Change PC62 and PC63 from 33uF to 470uF(to improve the CPU transient) B-19 : - P40 Movie PR180 and PR185 (to enhance remote sense) B-20 : - P30 dummy R1023, R1024, R1025, R1026 for impedance no match. B-21 : - P36 Change PR84 to 665 and PR342 to 4K for load line and OCP of CPU portion . B-22 : - P40 Change PR186 from 909 to 750 for OCP of VGA portion. B-23 : - P24 Add footprint(H44) : spad-qu5-3np for screw pad. B-24 : - P25 to reserve AC76,AC77,AC82,AC83 from 10UF to 1UF B-25 : - P14 VY1 P/N change to BG627000035. B-26 : - P26 Y9 P/N chane to BG625000081. B-27 : - P8 Y5 P/N chane to BG625000081. B-28 : - P30 R1027 ,R1028 ,R1029 & R1030 modify to dummy,for impedance no match. B-29 : - P24 Delete C1313 & C1314. B-30 : - P30 dummy C101 & C102. R847 & R848,For HDMI input capacitance value. B-31 : - P2 To reserve Q26 & R146,to solve leakage of DRAM_PWRGD. B-32 : - P25 To reserve Add AR70 & AR71,and to add AR72 & AR73 B-33 : - P30 dummy Q24, R770, R488, R487, R485, R482, R481, R478, R148, R144 @UMA for HDMI input VL.
C	03	-	5/29/12'	B - C C-01 : - P29 Del CN1, CN34, JSIM1, *R94, *C1054, *U54, *C1052, *C25 canel Japan TV C-02 : - P30 NA C249, C258 no need EMI solution C-03 : - P32 Add R1098, *R1099 Co-Lay re-driver C-04 : - P25 Add *AR75, *AR75 Reserve for HP C-05 : - P36 Change PR75 from 3.57K ohm to 3.6K ohm for CPU transient C-06 : - P24 add H45, H46 for Screw pad C-07 : - P36 Change PR342 to 3.65K for CPU transient C-08 : - P36 Change PR1036 to 680P, PR1039 to 56P for CPU transient C-09 : - P43 Change PC1017 to 68n for UMA transient